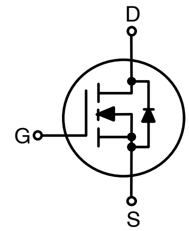
N-Channel Logic Level Enhancement Mode Field Effect Transistor

BSS123

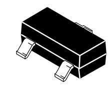


General Description

These N−Channel enhancement mode field effect transistors are produced using **onsemi's** proprietary, high cell density, DMOS technology. These products have been designed to minimize on−state resistance while provide rugged, reliable, and fast switching performance. These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

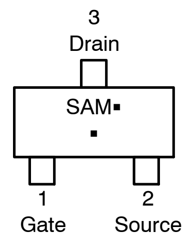
Features

- 0.17 A, 100 V
  - $R_{DS(on)}$ = 6 Ω @ V_{GS} = 10 V
  - $R_{DS(on)}$ = 10 Ω @ V_{GS} = 4.5 V
- High Density Cell Design for Extremely Low $R_{DS(on)}$
- Rugged and Reliable
- Compact Industry Standard SOT−23 Surface Mount Package
- This Device is Pb−Free and Halogen Free



SOT−23−3
CASE 318−08

MARKING DIAGRAM



SA = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
BSS123, BSS123−G	SOT−23−3 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted.

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain–Source Voltage	100	V
V_{GSS}	Gate–Source Voltage	±20	
I_D	Drain Current – Continuous (Note 1)	0.17	A
	Drain Current – Pulsed (Note 1)	0.68	
P_D	Maximum Power Dissipation (Note 1)	0.36	W
	Derate Above 25°C	2.8	mW/°C
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purposes, 1/16” from Case for 10 s	300	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS T_A = 25°C unless otherwise noted.

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction–to–Ambient (Note 1)	350	°C/W

ELECTRICAL CHARACTERISTICS T_A = 25°C unless otherwise noted.

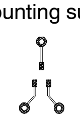
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	100	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	97	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 100 V, V_{GS} = 0 V	–	–	1	μA
		V_{DS} = 100 V, V_{GS} = 0 V, T_J = 125°C	–	–	60	
		V_{DS} = 20 V, V_{GS} = 0 V	–	–	10	nA
I_{GSS}	Gate–Body Leakage	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±50	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1 mA	0.8	1.7	2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 1 mA, Referenced to 25°C	–	–2.7	–	mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 10 V, I_D = 0.17 A	–	1.2	6	Ω
		V_{GS} = 4.5 V, I_D = 0.17 A	–	1.3	10	
		V_{GS} = 10 V, I_D = 0.17 A, T_J = 125°C	–	2.2	12	
$I_{D(on)}$	On–State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	0.68	–	–	A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 0.17 A	0.08	0.8	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	–	73	–	pF
C_{oss}	Output Capacitance		–	7	–	
C_{rss}	Reverse Transfer Capacitance		–	3.4	–	
R_G	Gate Resistance	V_{GS} = 15 mV, f = 1.0 MHz	–	2.2	–	Ω

ELECTRICAL CHARACTERISTICS T_A = 25°C unless otherwise noted. (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 30 V, I_D = 0.28 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	1.7	3.4	ns
t_r	Turn–On Rise Time		–	9	18	
$t_{d(off)}$	Turn–Off Delay Time		–	17	31	
t_f	Turn–Off Fall Time		–	2.4	5	
Q_g	Total Gate Charge	V_{DS} = 30 V, I_D = 0.22 A, V_{GS} = 10 V	–	1.8	2.5	nC
Q_{gs}	Gate–Source Charge		–	0.2	–	
Q_{gd}	Gate–Drain Charge		–	0.3	–	
DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain–Source Diode Forward Current		–	–	0.17	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.44 A (Note 2)	–	0.8	1.3	V
t_{rr}	Diode Reverse Recovery Time	I_F = 0.17 A, d_{if}/d_t = 100 A/µs	–	11	–	ns
Q_{rr}	Diode Reverse Recovery Charge		–	3	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) 350°C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%

TYPICAL CHARACTERISTICS

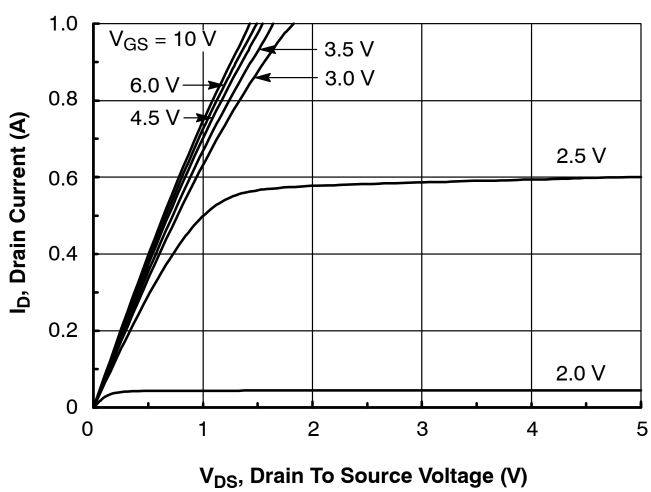


Figure 1. On–Region Characteristics

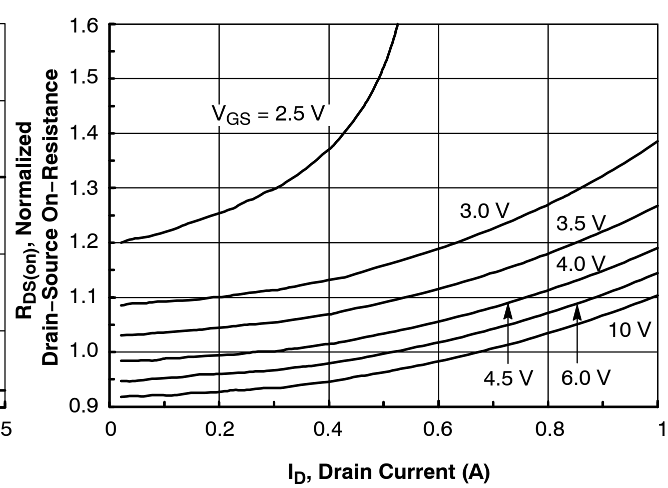


Figure 2. On–Resistance Variation with Drain Current and Gate Voltage

TYPICAL CHARACTERISTICS (continued)

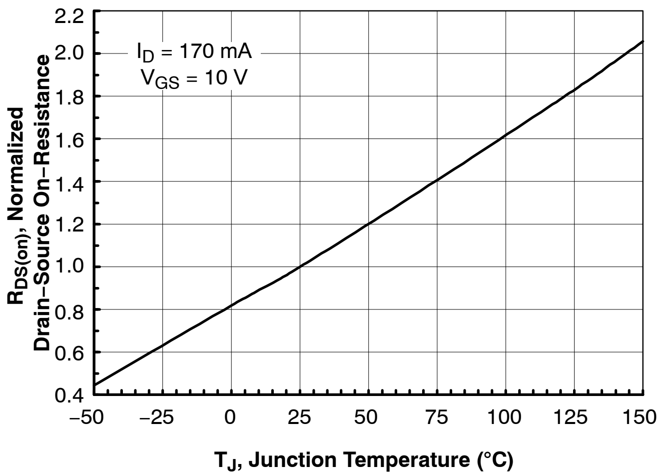


Figure 3. On−Resistance Variation with Temperature

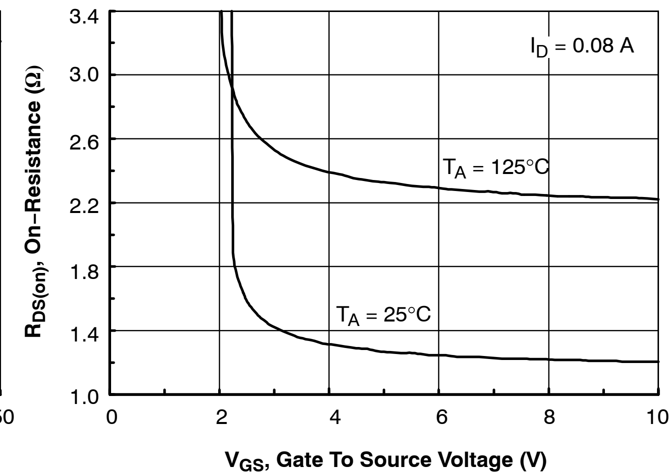


Figure 4. On−Resistance Variation with Gate−to−Source Voltage

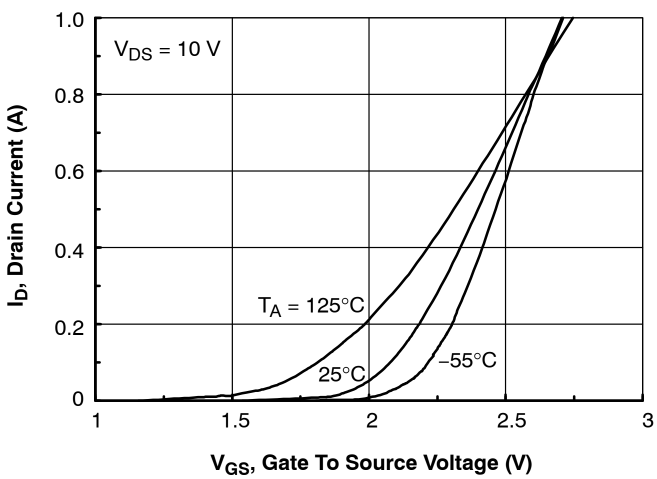


Figure 5. Transfer Characteristics

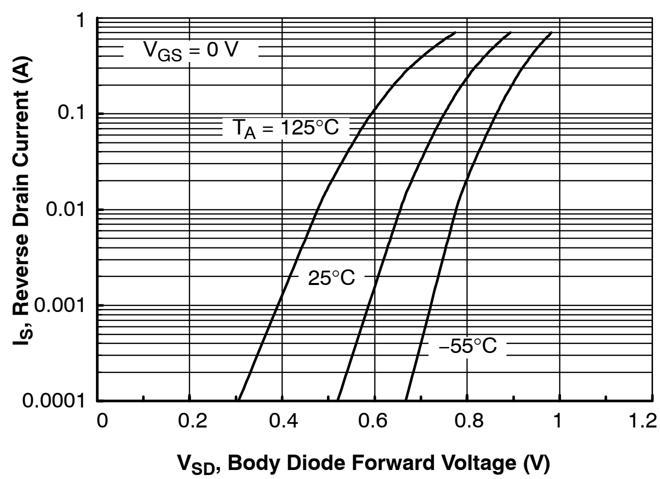


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

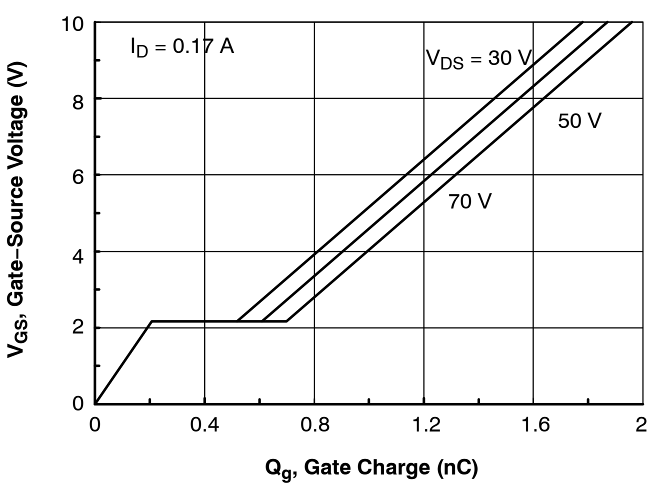


Figure 7. Gate Charge Characteristics

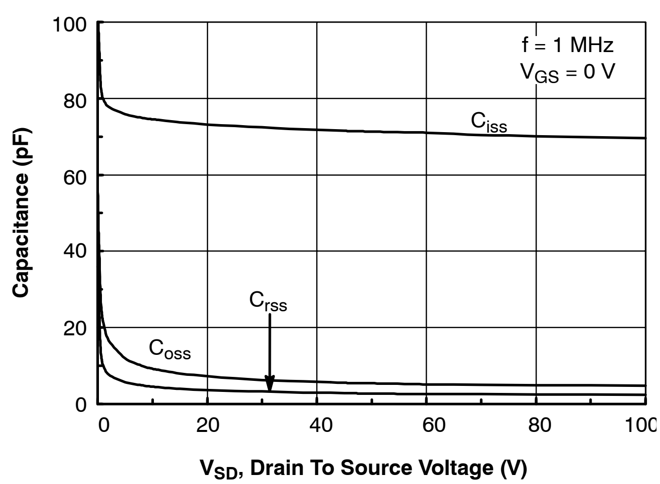


Figure 8. Capacitance Characteristics

TYPICAL CHARACTERISTICS (continued)

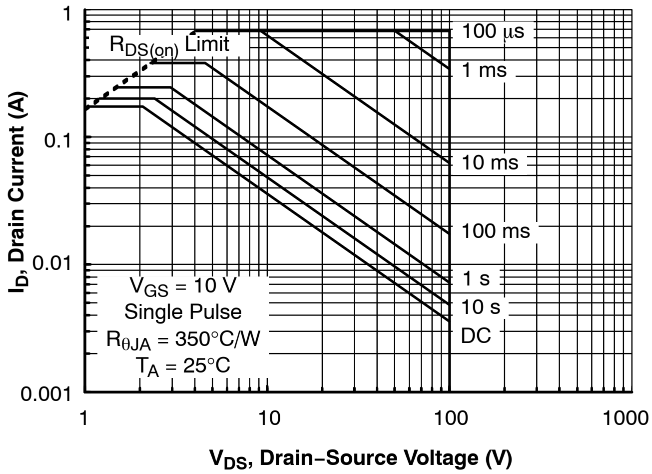


Figure 9. Maximum Safe Operating Area

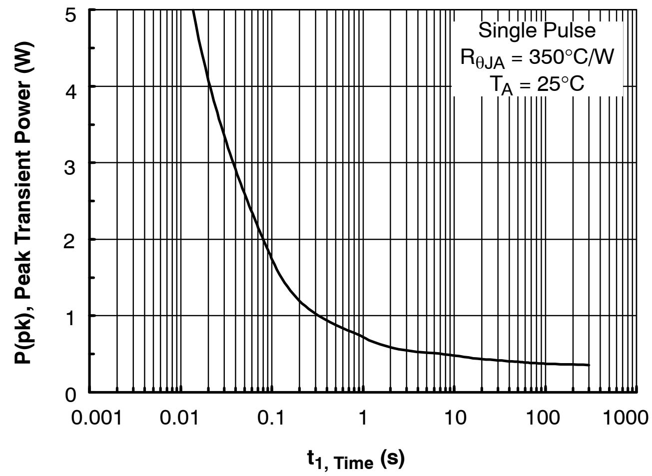


Figure 10. Single Pulse Maximum Power Dissipation

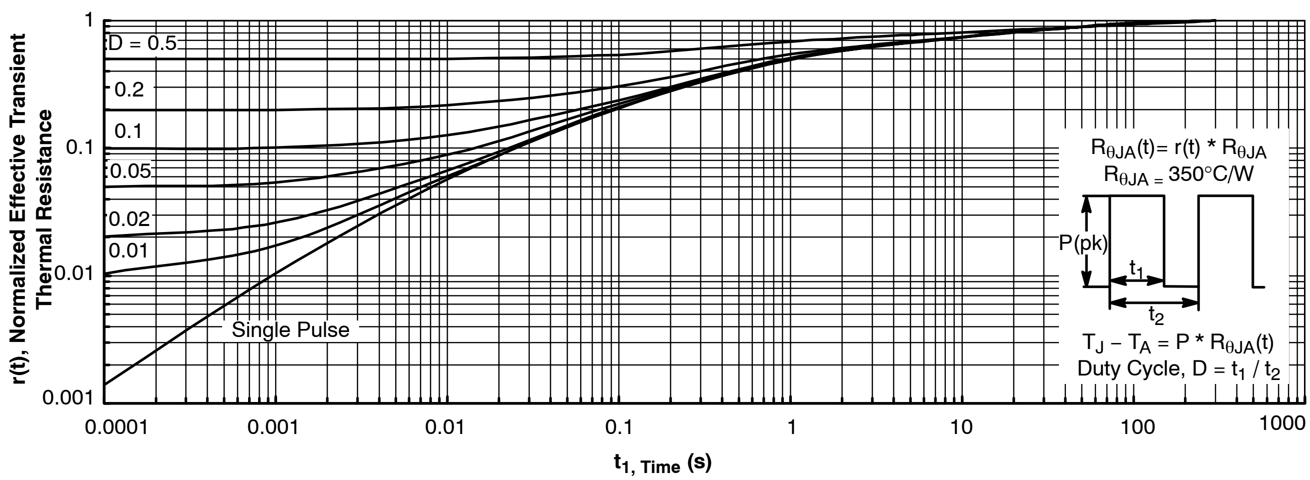
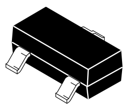


Figure 11. Transient Thermal Response Curve

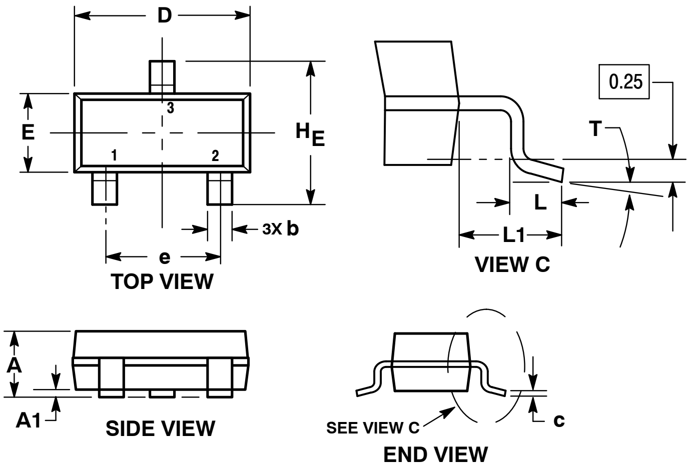
Thermal characterization performed using the conditions described in Note 1a.
Transient thermal response will change depending on the circuit board design.



SCALE 4:1

SOT−23 (TO−236)
CASE 318−08
ISSUE AS

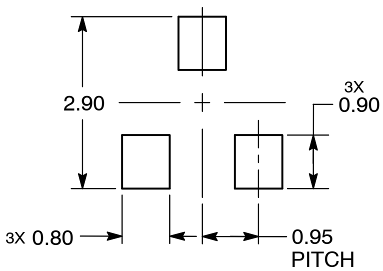
DATE 30 JAN 2018



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

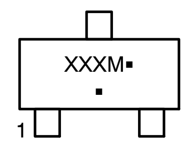
	MILLIMETERS			INCHES		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H_E	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	−−−	10°	0°	−−−	10°

RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

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DESCRIPTION:	**SOT−23 (TO−236)**	**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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For additional information, please contact your local Sales Representative

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