Test and Design for Testability of Analog and Mixed-Signal Circuits

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Test is critical

- Semiconductor industry is extremely competitive and is asking for the best quality and reliability levels at the lowest cost.
- Nanoscale devices in combination with gigascale complexity
- Increasing complexity (e.g., more than 100 microcontrollers in one car)
- Test is becoming a dominant factor in overall manufacturing cost.
- Long product life times, typically from 10 to 25 years (!), which require zero reliability defect

Test is critical

- Harsh and/or variable environment (e.g., in a car or in a human body)
- Heterogeneous systems (MEMS, RF, digital, etc.) in miniaturized packages
- Mandatory secure communication links (data integrity, protection against attacks)
- Complex diagnosis and very high costs or risks of maintenance/repair (e.g. implanted devices)
- Test is the last chance to deliver quality and reliability to the end customer!

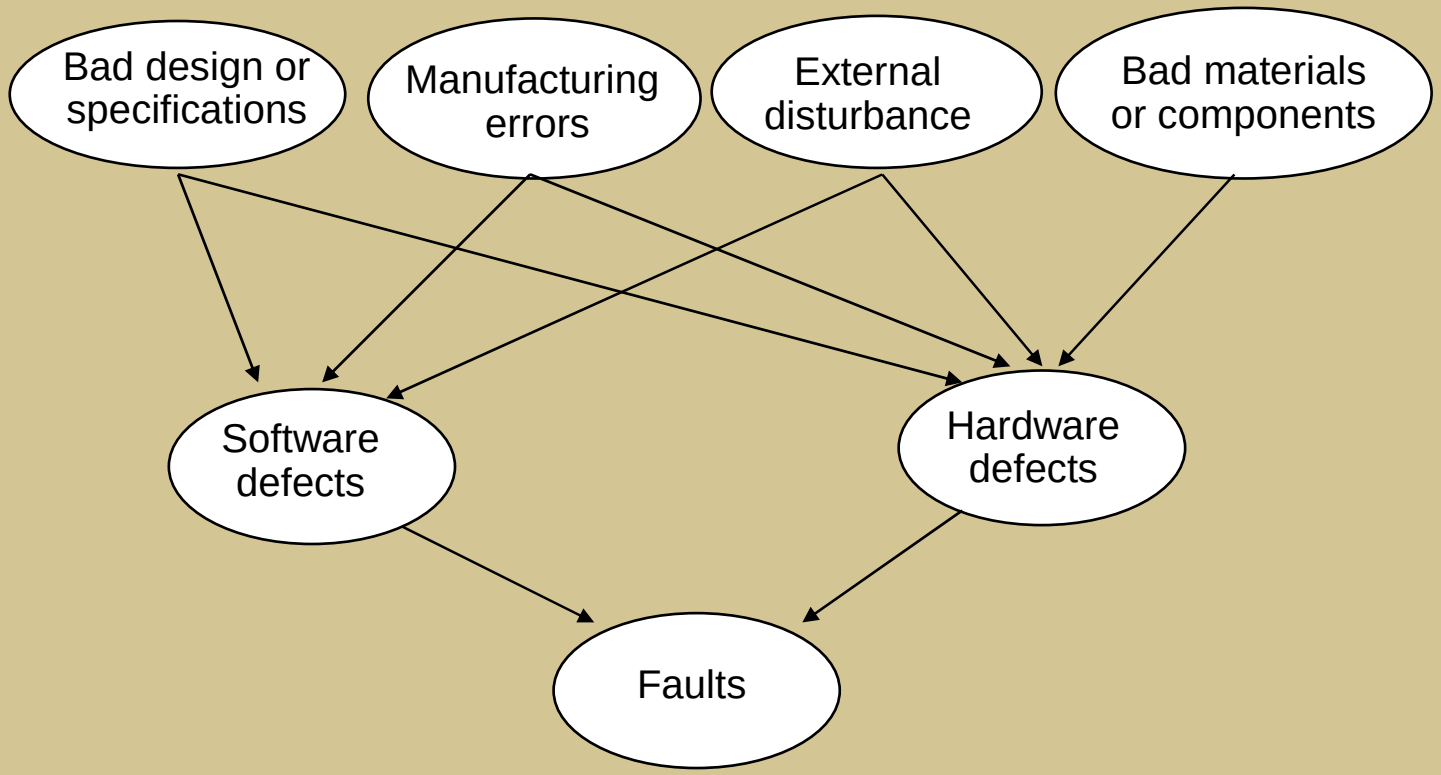
Outline

- Basic concepts on testing and design for testability
- Defect, fault modeling and test metrics
- Design for testability and built-in self-test
  - structural and functional test
- Standard test infrastructures
- Digital signal processing based testing

Basic concepts

on Testing and Design for Testability

- "Our reason for living"



Basic concepts

on Testing and Design for Testability

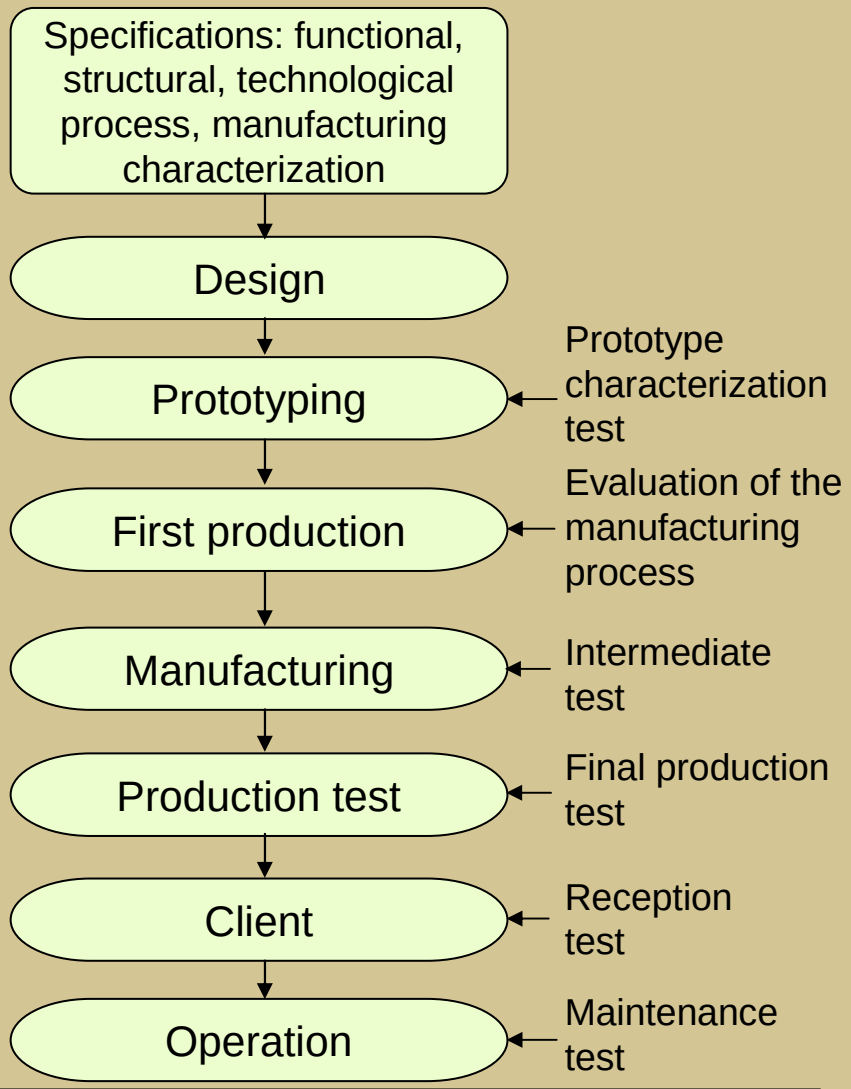
Product life-cycle (value chain)

The test of an IC can occur in different stages:

- at the wafer level

(*probing the wafer*)

- after packaging
- after insertion in a board
- as part of a system
- as part of a system operating in the field



Basic concepts

on Testing and Design for Testability

Types of test

Production: Wafer Sort /Probe Final / Package	Tests of manufactured parts to sort out those that are faulty; Test of each die on the wafer; Test of packaged chips and separation into bins (military, commercial, industrial)
Design verification	Verification of design correctness
Characterization or Engineering	Determine actual values of devices' Ac and Dc parameters and interaction of parameters: Set final specifications and identification of possible process yield improvement.
Quality / Sample	Test a sample of each lot of manufactured parts.
Go / No Go	Determine whether devices meet specifications
Stress Screening (ESS/Burn-in)	Test under high temperature, temperature cycling, vibration, .., to eliminate short life parts
Reliability (Accelerated life)	Estimate time to failure in normal operation after operation under high temperature
Diagnostic / Repair	Identify failures and locate defects
Acceptance	Demonstrate / verify degree of compliance with specified requirements
On-line / checking	Verification of operation correctness during normal operation

Basic concepts

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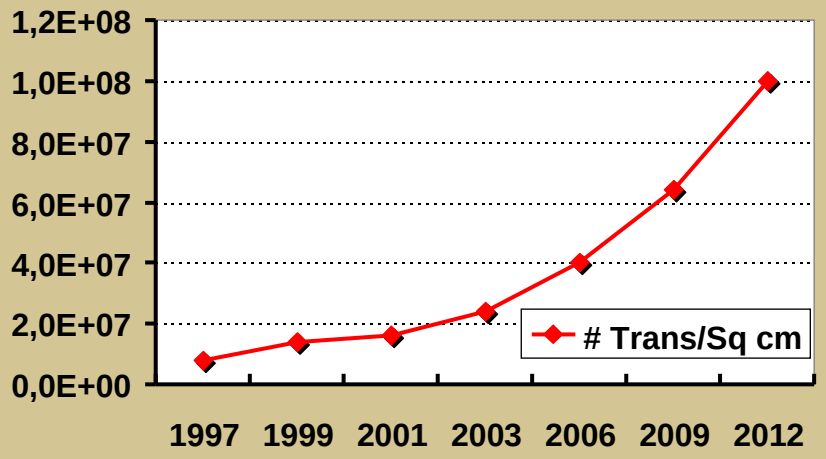
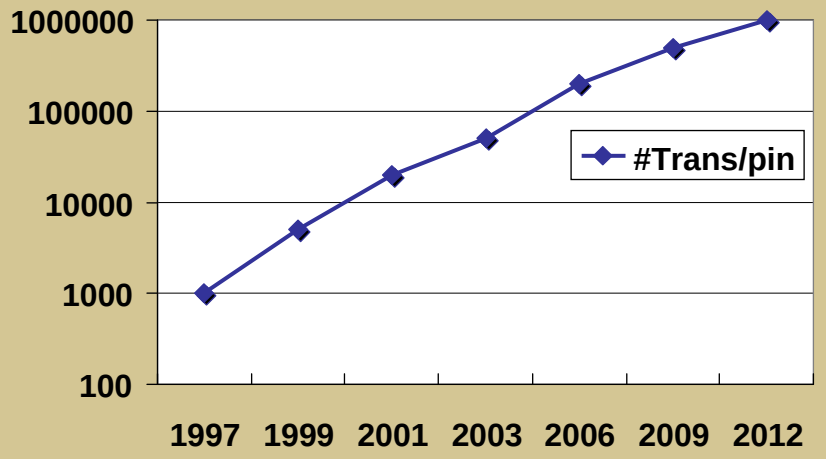
Test Complexity

Test development and application time may become prohibitive





Basic concepts

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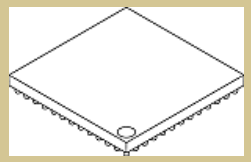
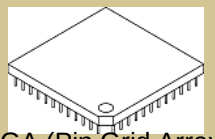
New packaging types

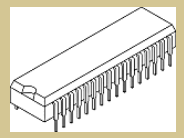
Package inductance:
1 - 5 nH



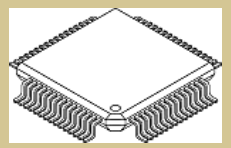
BGA (Ball Grid Array)



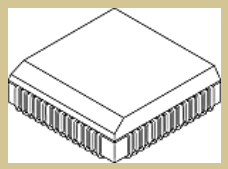
PGA (Pin Grid Array)



DIL (Dual In Line)

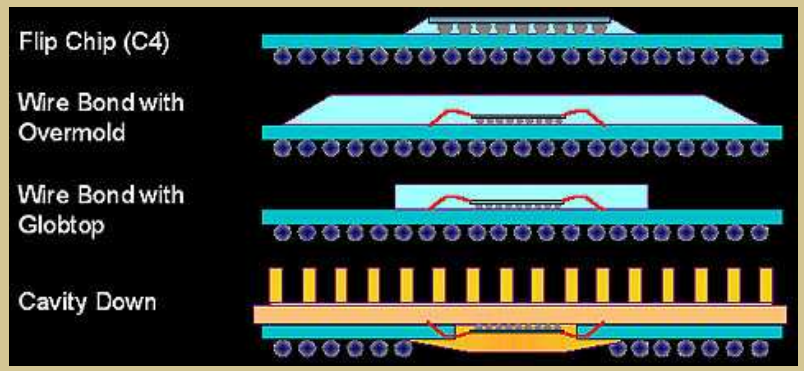


QFP (Quarter Flat pack)



PLCC (Plastic leaded chip carrier

- BGA (Ball Grid Array)
  - Small solder balls to connect to board
  - small
  - High pin count
  - Cheap
  - Low inductance
- CSP (Chip scale Packaging)
  - Similar to BGA
  - Very small packages



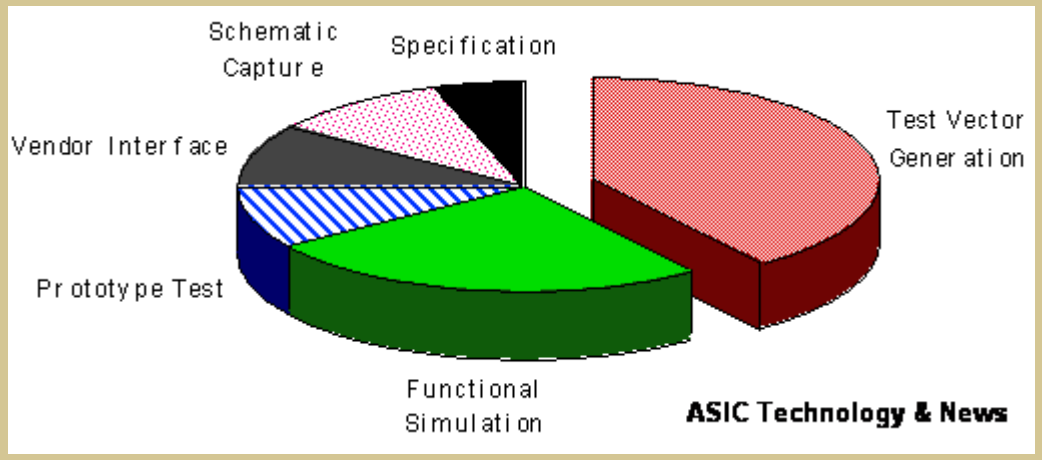
Basic concepts

on Testing and Design for Testability

- "*AMS circuits account for 70% of SOC-test cost and 45% of test-development time, even though they make up a small fraction of the chip complexity*,"

  Karim Arabi, Qualcomm

- Test pattern generation can account for 40 % of an ASIC design time



Basic concepts

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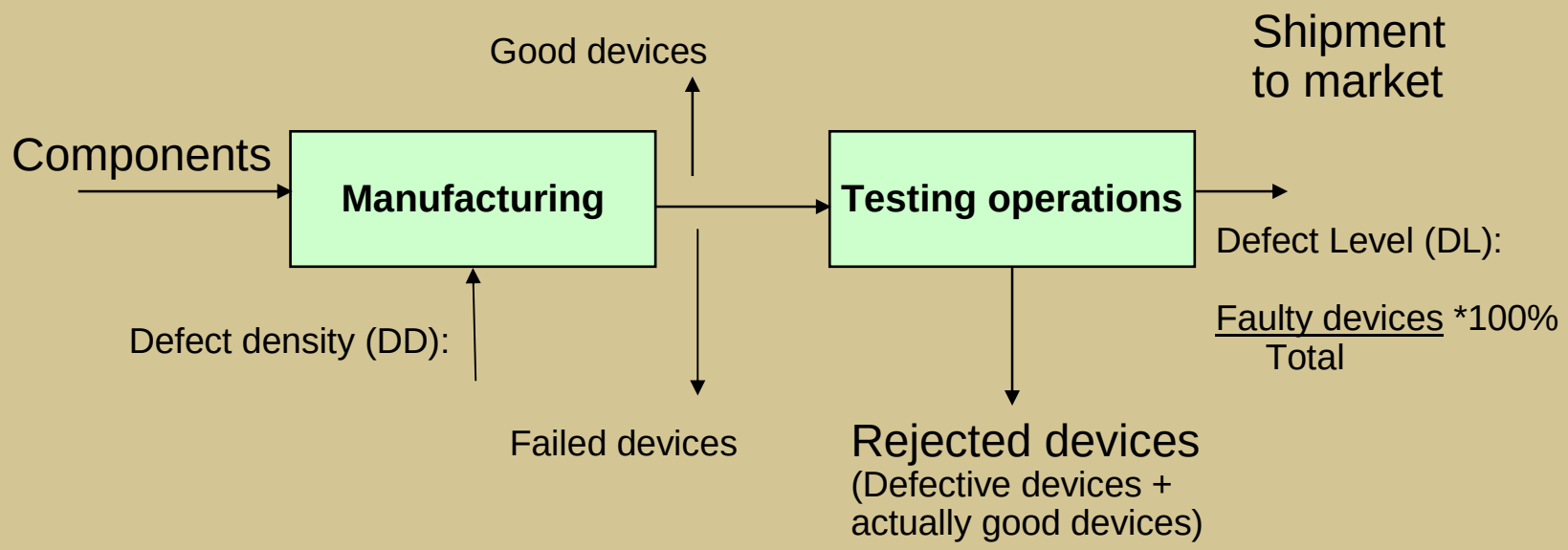
- Testing – process of screening/detecting defective parts (in a manufacturing line)

Production Yield (Y) $Y = \frac{N_{PassedDevices}}{\#TotalDevices} \times 100\%$



Basic concepts

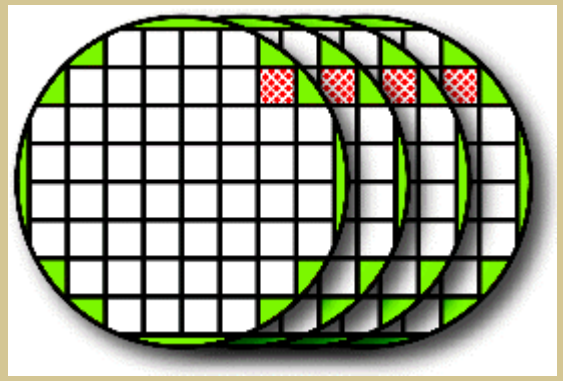
on Testing and Design for Testability

Yield — production efficiency: measures the percentage of good components in the overall production volume – a statistical parameter.

$$Y = e^{-DD.SA}$$

$$N_{PassedDies} = N_{Dies/Wafer} . N_{Wafers/Lot} . Y$$

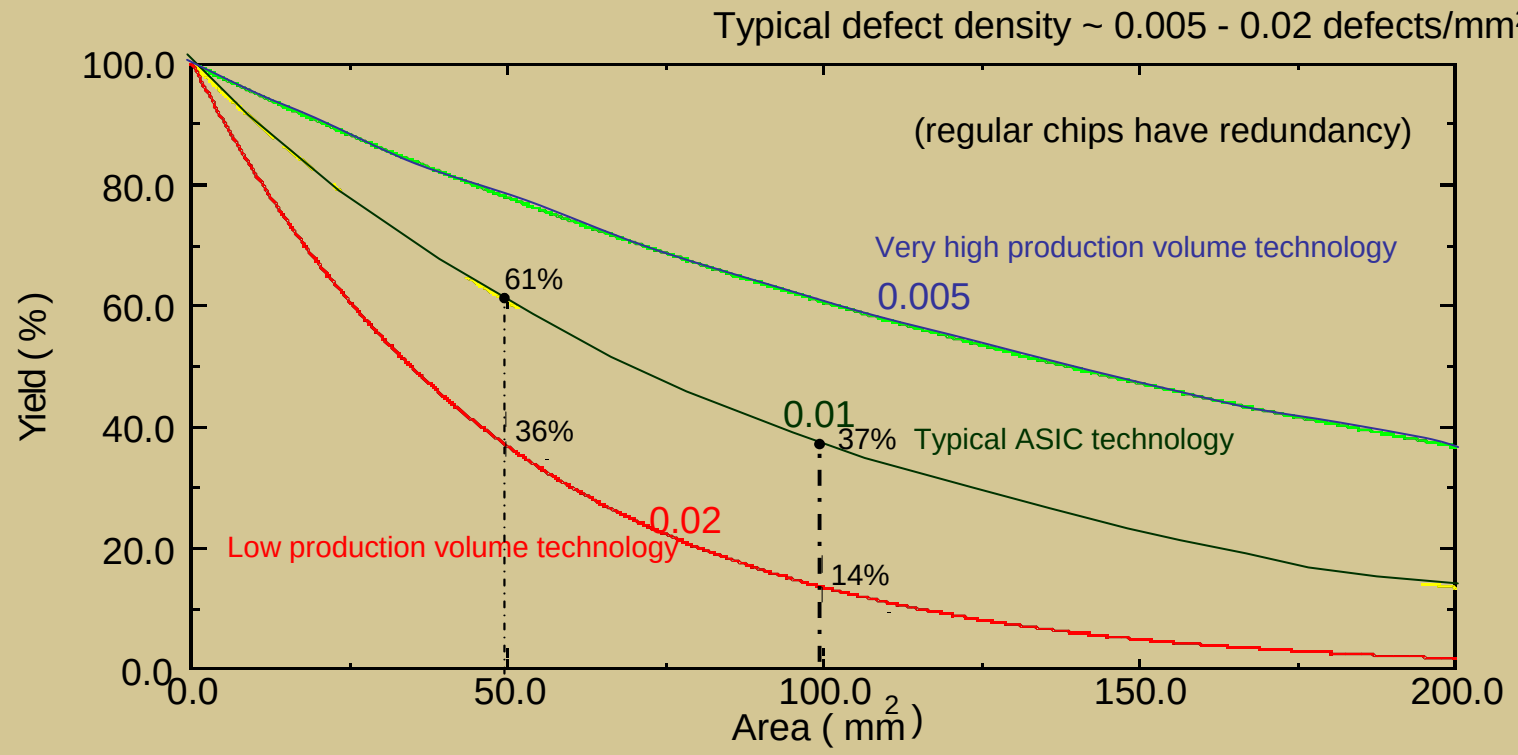
$$N_{FailedDies} = N_{Dies/Wafer} . N_{Wafers/Lot} . (1 - Y)$$



Basic concepts

on Testing and Design for Testability

Production yield $Y = e^{-Area*DefectDensity}$



Price of 100 mm^2 chip compared to 50 mm^2 chip: 100 mm^2/50 mm^2 x 0.61/0.37 = 3.4 (D=0.01)

100 mm^2/50 mm^2 x 0.36/0.14 = **5.3** (D= 0.02)

Basic concepts

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Testing time

$$T_{test_{chip}} = \frac{T_{setup} + T_{wafer_{loading}} \times NWL + T_{die_{stteping}} \times NDW \times NWL + T_{pass} \times NPD + T_{fail} \times NFD}{NDW \times NWL}$$

$$Cost_{test} = T_{test_{chip}} \times Test_{CostRate}$$

$$Test_{CostRate} = (D_{Tester} + D_{Handler} + C_{Fixed}) \left(\frac{T_{test\ allchips}^{T_{Total}} + T_{Handler}}{T_{test\ allchips}} \right) \left(\frac{T_{TesterUsed} + T_{Down} + T_{Idle}}{T_{TesterUsed}} \right)$$

$$Throughput = \frac{N_{good\ devices}}{T_{Total}}$$

Basic concepts

on Testing and Design for Testability

Classes of IC Electrical Tests

- Functional
  - Detection of failures by verification of correct operation rather than by verifying the absence of specific faults
  - Verification that circuits operate correctly and meet specifications (*design verification*)
- Structural (DC parametric tests) – test for the occurrence of faulty behaviours; interconnections; presence of protection circuits
- AC, parametric tests
  - Measure of time parameters, leakage currents, power consumption

Basic concepts

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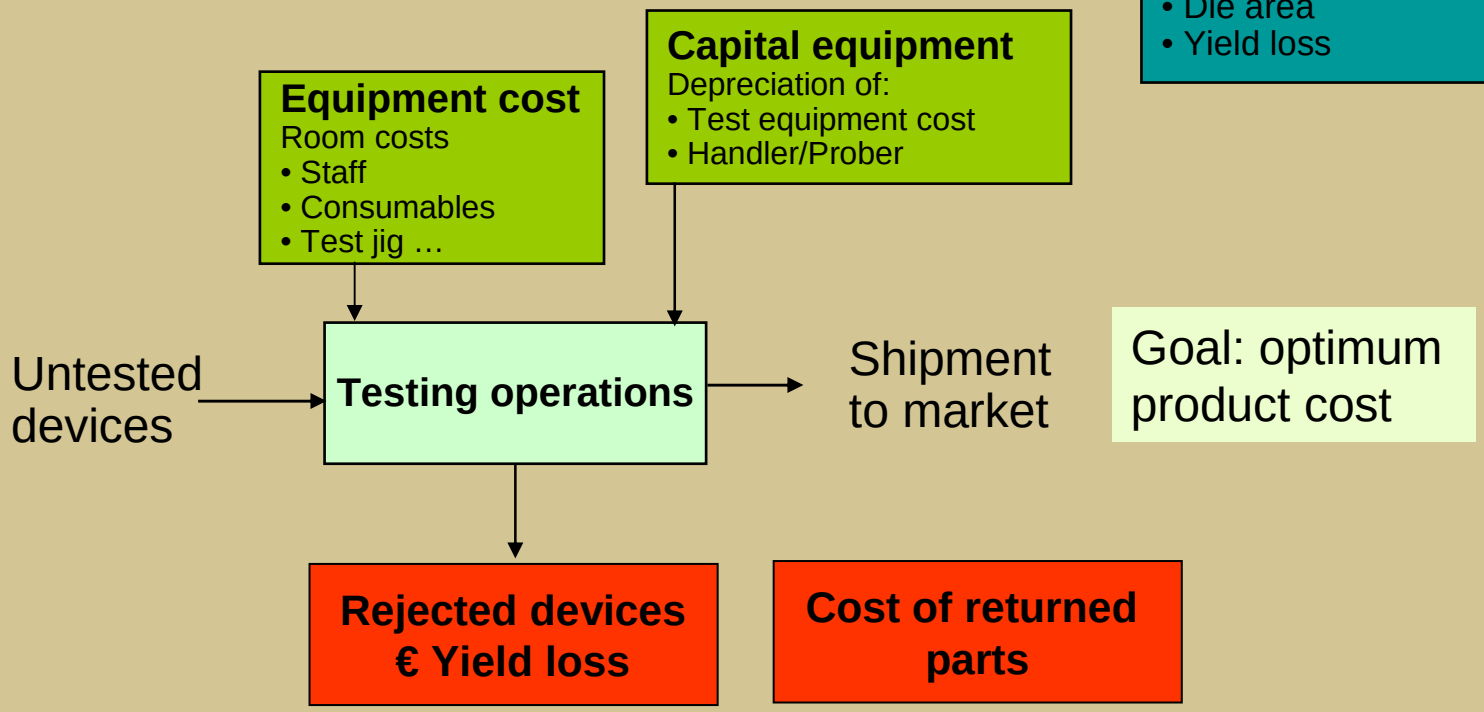
Test Cost

NRE Costs
- DfT design and validation cost
- Test generation cost

Device costs
- Die area
- Yield loss



Basic concepts

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- Costs
  - C_{dftde}: DfT design effort
  - C_{dftt}: DfT tools
  - C_{atpg}: ATPG development
  - C_{ap}: Test application
  - C_{esc}: Test escapes
  - C_{ohd}: Silicon overhead
  - C_{pr}: Performance loss
  - C_{yl}: Yield loss
- Benefits
  - C_{tm}:Time to market
  - C_{va}:Verification ability
  - C_{ned}-C_{ed}: Test escape diagnosis

Basic concepts

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$$ROI = \frac{Benefit}{Cost + C_{esc}}$$

$$Benefit = \frac{C_t}{N_{gd}} + \frac{C_{va}}{N_{gd}} + (C_{ned} - C_{ed})$$

$$Cost = \frac{C_{atpg}}{N_{gd}} + C_{ap} + C_{esc} + C_{ohd} + C_{pl} + \frac{C_{yl}}{N_{gd}}$$

$$C_{esc} = C_{bd} + C_{sd} + C_{fs}$$

$$C_{bd} = K_{loop} \times T_{bd} \times C_{labor} \times N_{icb} \times P_{bd}$$

$$C_{sd} = T_{sys} \times C_{labor} \times N_{sys} \times P_{sys}$$

$$C_{fs} = \left(T_{fs} \times C_{labor} + C_{spare} + C_{travel} + C_{downtime}\right) \times N_{sys} \times P_{fs}$$

Basic concepts

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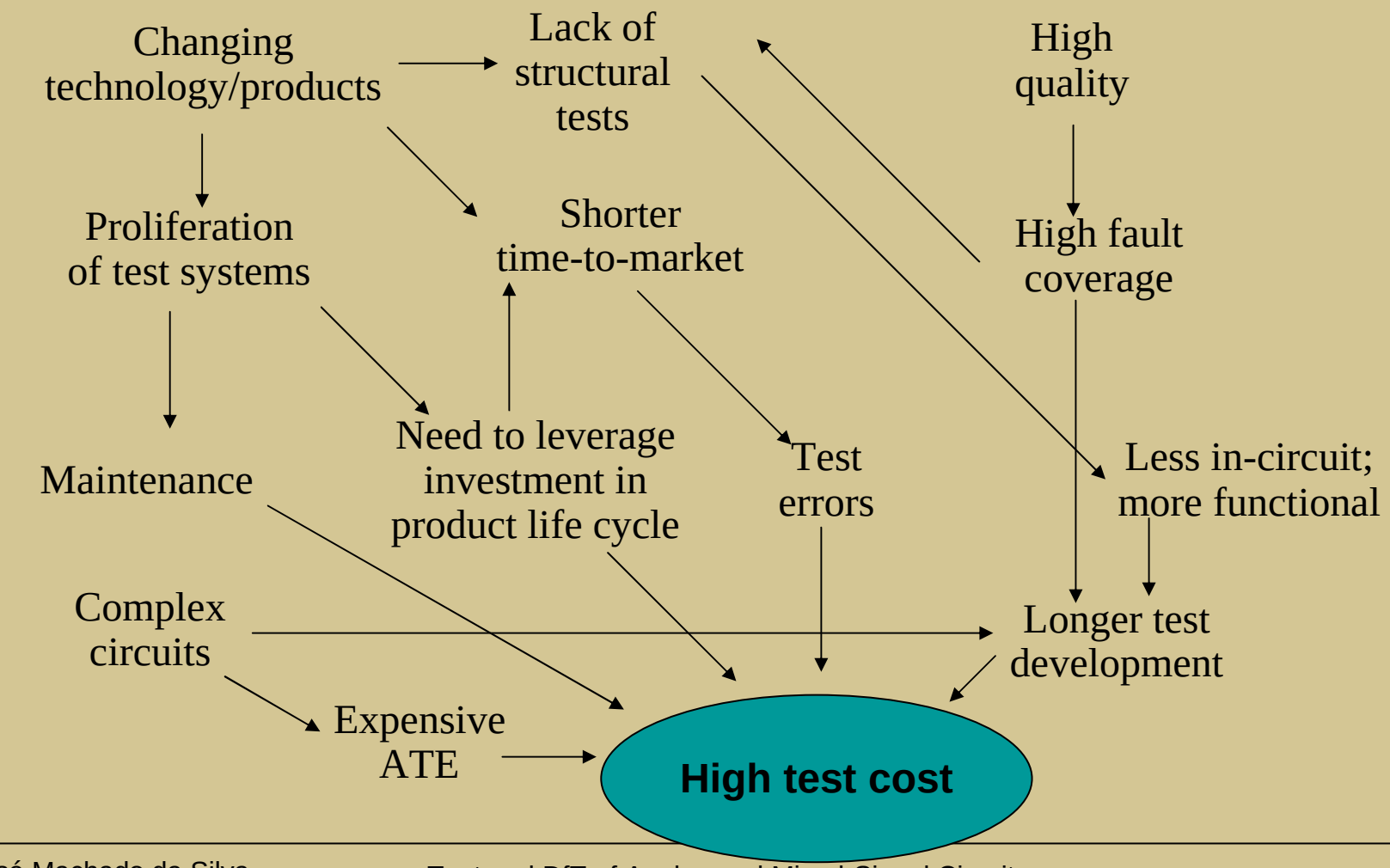
Aspects affecting test cost



Basic concepts

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- Manufacturer A (MA)
  - 150000 boards/year; 28 $/ board
  - 800 components; 4000 solder joints / board
  - Board repair yield: 85%, up to 5 repair cycles; scrapt rate: 0,0076%
  - Electrical defect rate: 250 defects per million (DPM); average 0,2 defects/board
  - Structural defect rate: 400 DPM; average 1,6 defects/board

Basic concepts

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	ICT	FT	ESS	System
Labor cost of Verification/Diagnosis [$/h]	2	2	2	2
Repair labor cost [$]	2	2	2	2
Diagnostics/verification time per defect [min]	5	10	60	120
Repair time per defect [min]	15	30	50	50
Debug/diagnosis cost per defect [$]	0,17	0,33	2	4
Repair cost per defect [$]	0,5	1	1,67	1,67
Retest cost [$]				
Field failures/returns cost - $2				
Current field return rate - 0,02 %				

Basic concepts

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Test Coverage Assumptions	ICT 1	ICT 2	FT	ESS	System
Test access [%]	95	95	50	70	80
Fault coverage structural [%]	80	85	60	90	60
Fault coverage electrical [%]	90	95	85	95	99
Test coverage [%]	78	82	32	64	53
False fail rate [ppm]	50	25	10	5	2

Basic concepts

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Total test costs, ICT 1	ICT 1	FT	ESS	System	
Structural defects before test [per board]	1,600	0,3840	0,26880	0,09946	
Structural defects after test [per board]	0,384	0,2688	0,09945	0,05172	
Electrical defects before test [per board]	0,200	0,0290	0,01668	0,00559	
Electrical defects after test [per board]	0,029	0,01668	0,00559	0,00116	
Structural defects found [per board]	1,216	0,1152	0,16930	0,04770	
Electrical defects found [per board]	0,171	0,0123	0,01110	0,00440	
Total defects found [per board]	1,387	0,1275	0,18040	0,05220	
First pass yield [%]	25	88	83,5	94,9	
Overall test effectiveness [%]	77	31	63	50	
DPM remaining on board after test	86	59.5	21.9	11	**Total**
Annual verification costs [$]	34.675	6.376	54.13	31.298	126.479
Annual repair costs [$]	104.025	19.129	45.108	13.041	181.303
Annual scrap costs [$]	741	80	93	28	943
Annual retest cost [$]	56.263	17.959	49.527	15.248	138.998
Annual field failure/return costs [$]					6000
Total [$]	139.441	25.585	99.331	44.367	453.722

Basic concepts

on Testing and Design for Testability

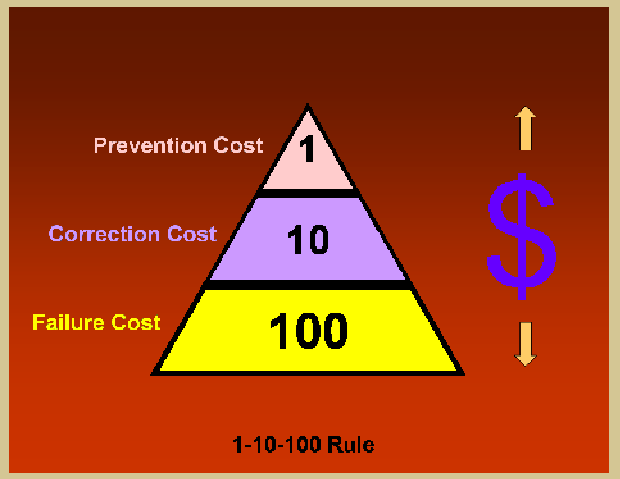
Total test costs, ICT 2	ICT 2	FT	ESS	System	
Structural defects before test [per board]	1,600	0,3090	0,21560	0,07980	
Structural defects after test [per board]	0,308	0,2156	0,07980	0,04150	
Electrical defects before test [per board]	0,200	0,0195	0,01120	0,00376	
Electrical defects after test [per board]	0,020	0,01120	0,00376	0,00078	
Structural defects found [per board]	1,292	0,0924	0,13580	0,03830	
Electrical defects found [per board]	0,171	0,0123	0,01110	0,00440	
Total defects found [per board]	1,473	0,1007	0,14330	0,04130	
First pass yield [%]	22,9	90,4	86,7	96	
Overall test effectiveness [%]	82	31	63	49	
DPM remaining on board after test	68,2	47,3	17,4	8,8	**Total**
Annual verification costs [$]	36.813	5.034	42.985	24.759	109.591
Annual repair costs [$]	110.438	15.103	35.821	10.316	171.678
Annual scrap costs [$]	726	68	76	23	893
Annual retest cost [$]	57.799	14.368	40.048	12.128	124.342
Annual field failure/return costs [$]					4.795
Total [$]	147.976	20.205	78.883	35.099	411.299
				Savings	**42.423**

Basic concepts

on Testing and Design for Testability

The 1:10:100 Rule:

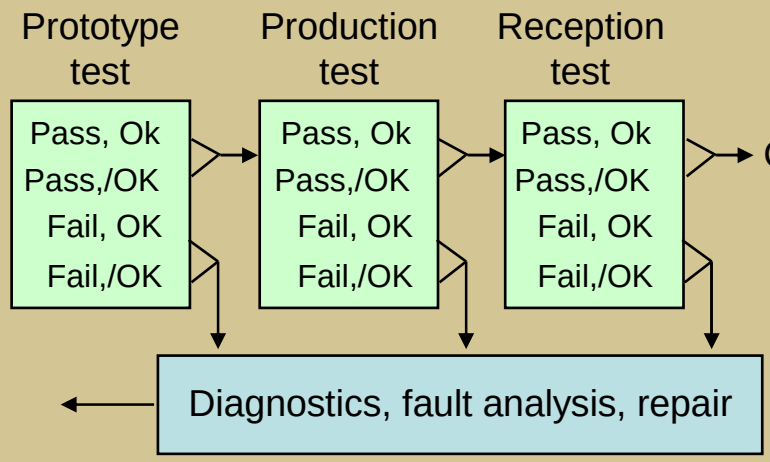
- The **cost** to **fix** a **defect increases exponentially** the later in the development lifecycle that it is identified.
- A defect caught in requirements phase costs a factor of 1 (1x) to fix.
- A defect caught in construction costs 10 times as much as in requirements.
- A defect caught in production costs up to 100 times as much as in requirements.



Basic concepts

on Testing and Design for Testability

- Test metrics



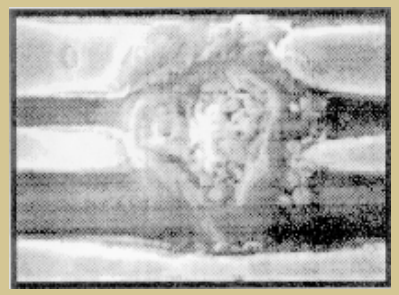
$$D_{efectLevel} = \frac{Pass/Ok}{Pass/Ok + PassOk}$$

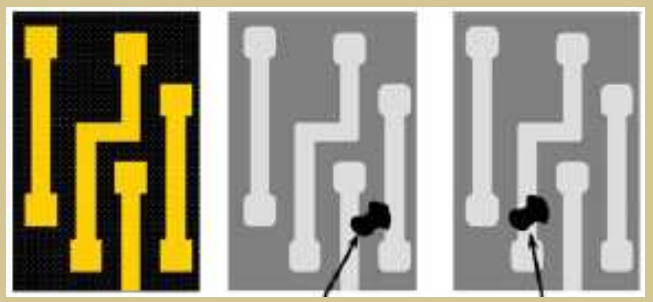
Progress in Design for Test: A Personal View
R. G. Bennets. IEEE Design and Test of Computers, Spring 1994

Defect, fault modeling and test metrics

Typical defects

- Open circuits, high contact resistance and short-circuits in and among different layers
- Threshold voltage, transconductance, aspect ratio deviations
- Gate-oxide shorts, metallization failures or corrosion
- High leakage currents
- Defective bonding or packaging, geometry deviations
- Parasitic transistors
- Hot electrons, cosmic radiation, α particles
- Electromigration

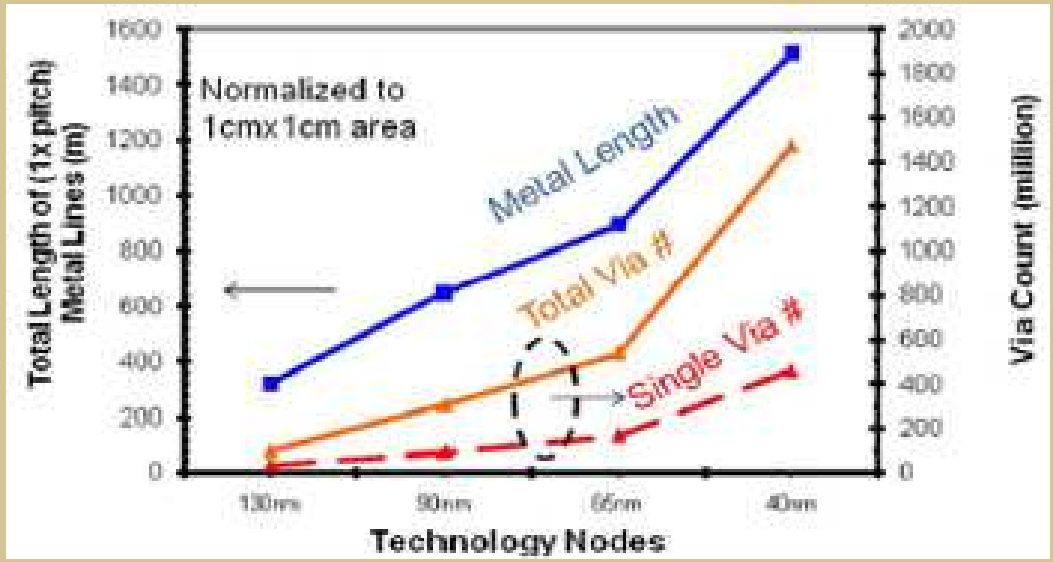




Defect, fault modeling and test metrics

- Nvidia Corp 40 nm graphics processor has 3.2 billion transistors and 7200 million vias (> world population)
- via deposition is a major reliability concern.
- leakage power has "become almost intolerable“, “DC power has exceeded AC power for the first time,"
- the needs for zero defects and zero variability have become paramount.

John Chen, Nvidia Corp

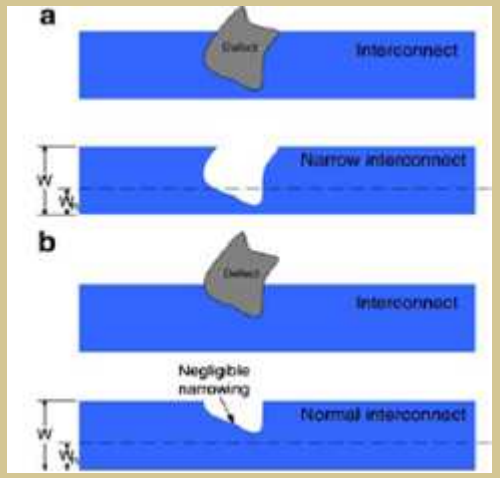


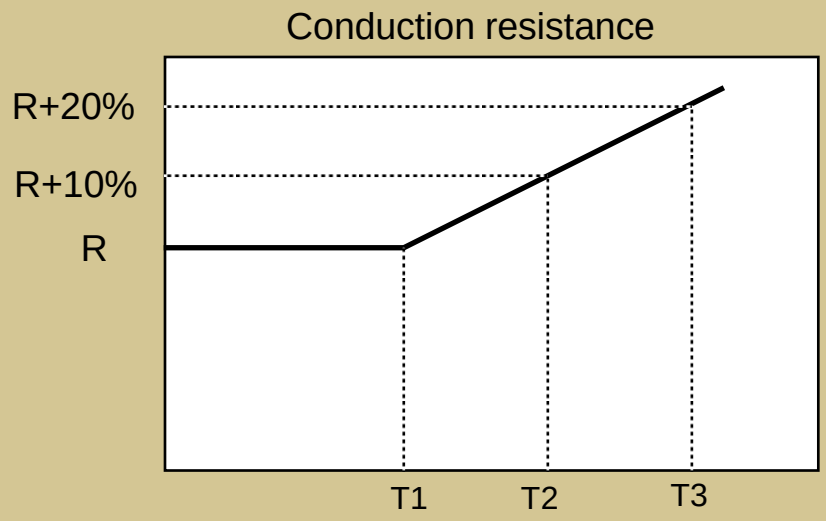
Defect, fault modeling and test metrics

- **Electromigration**

Aggravated by:

  - Reduction of the metallic interconnection width
  - Reduction of contact area
  - Higher current densities





Defect, fault modeling and test metrics

In terms of duration defects can be:

- Permanent – their effect remains after the first occurrence
- Intermittent – their effect occur in intervals
- Transient – their occurrence is triggered by a particular event and whose effect is temporary (e.g., cross-talk)

Physical defects are not manageable with common simulation tools.

That requires their representation with fault models.

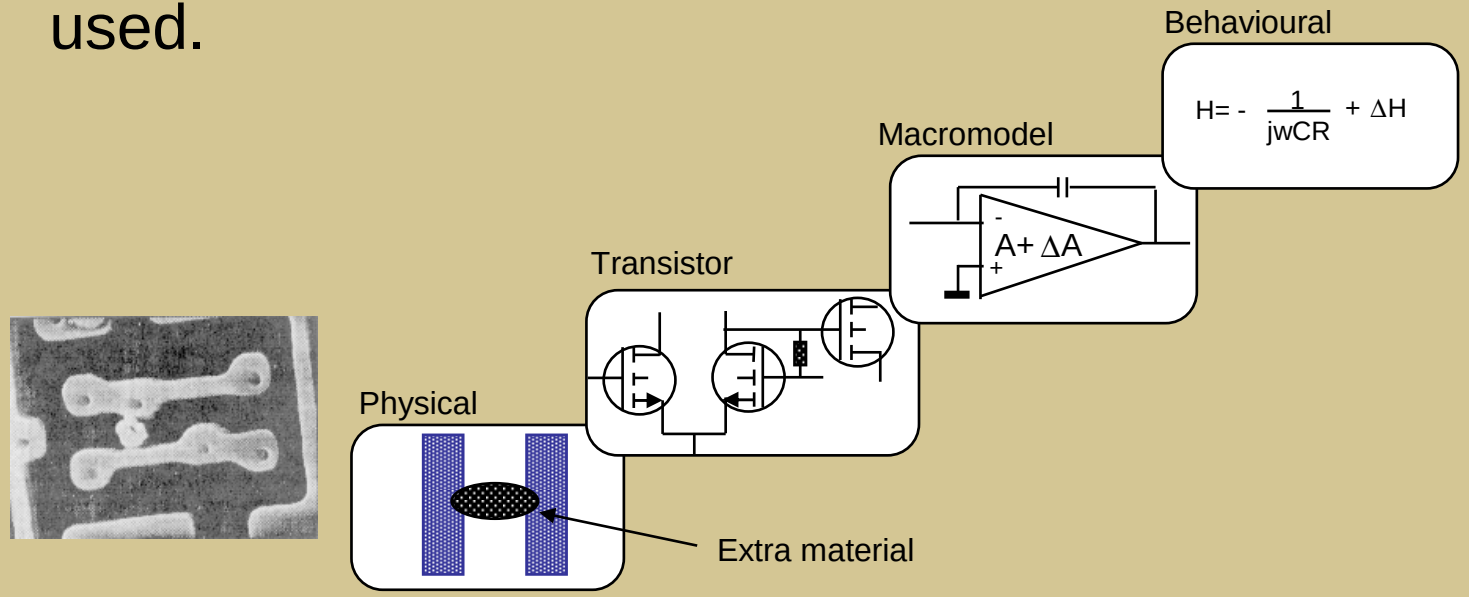
Defect, fault modeling and test metrics

Fault model

- The translation of a defect into the electrical or logic level.
- A formal representation of the mode how the physical defect affects/changes a circuit's behaviour in a certain level of abstraction.
- Knowing the physical mechanisms behind the occurrence of a defect, and how these manifest electrically is fundamental to develop realistic fault models. These are required for test stimuli generation and to evaluate tests quality.

Defect, fault modeling and test metrics

The same defect can be represented by different fault models according to the level of abstraction being used.



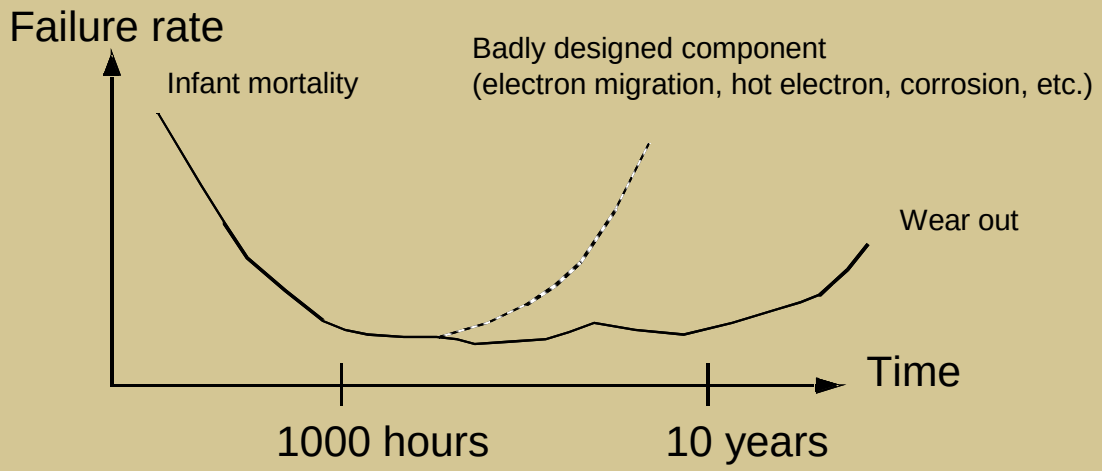
Attributes of a good fault model

Simplicity, to allow efficient test vector generation and fault simulation procedures

Defect coverage, to guarantee that the percentage of defective components escaping detection is acceptably low

Defect, fault modeling and test metrics

Reliability



- Failing parts within first 1000 hours: 1 - 5 %
- Burn-in testing : Heating up chips to 125 deg. accelerates 1000 hours period to approx. 24 hours.
  - Static: power supply connected
  - Dynamic: Power + stimulation patterns.
  - Functional test: Power + stimulation patterns + test.
- Temperature cycling: continuous temperature cycling of chips to provoke temperature gradient induced faults. (Non matching thermal expansion coefficients).
- Electrical stress: Operation at elevated supply voltage
- I_{DDQ}

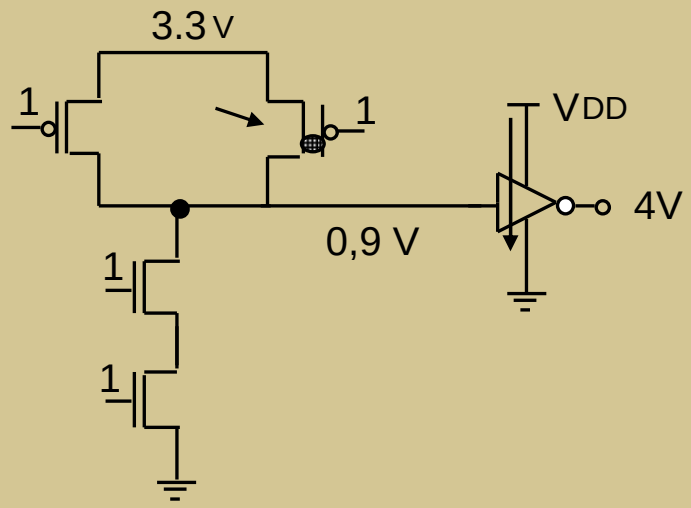
Defect, fault modeling and test metrics

I_{DDQ} Test - Improved Process Control

Set CMOS devices into static state and measure tiny current leaking from power to ground

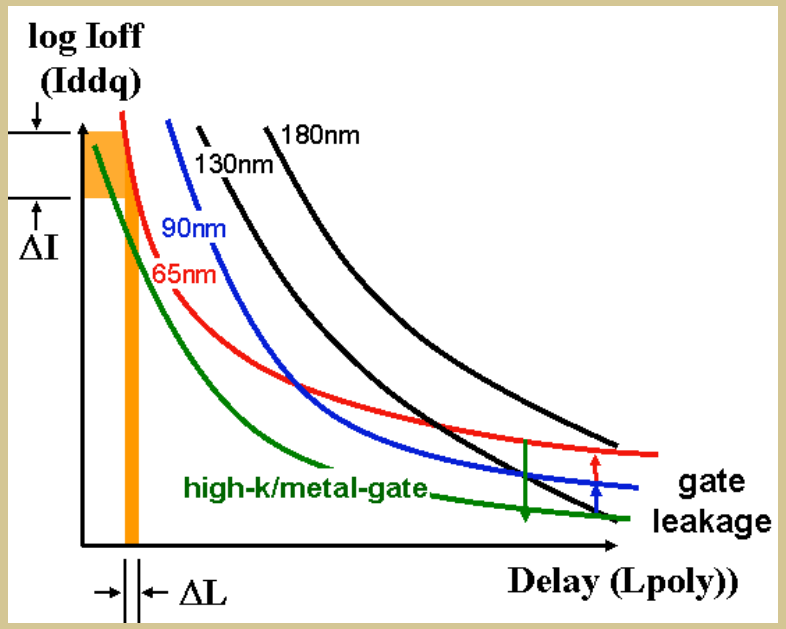
- Certain defects are easily detected after the observation of the quiescent power supply current - **I_{DDQ}**.

- A resistive defect which may fail in the customers device
  - Excessive I_{DDQ} signals the presence of leakage currents which are an indicator of process problems and reliability issues on medium/long term.



Defect, fault modeling and test metrics

- I_{DDQ} testing can only be performed if the device design is compatible, i.e. designed for test
- main requirements:
  - stable current at the moment of measurement
  - repeatable test conditions (substrate bias, temperature, VDD, …)



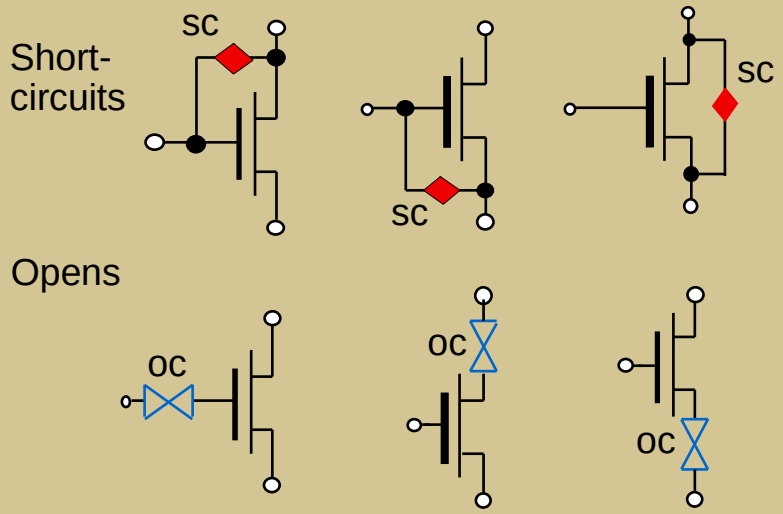
Shorter channel transistors exponentially contribute more to I_{DDQ}

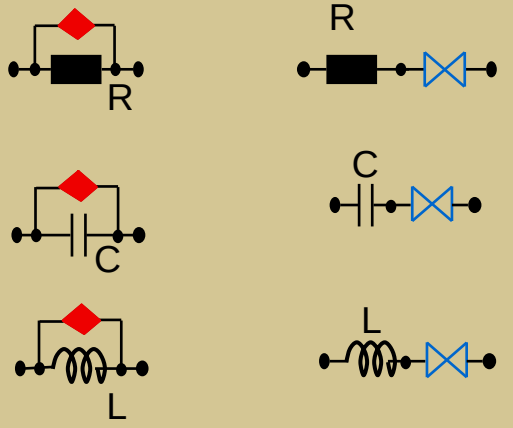
An Effective Design-for-Iddq-Testing Approach for Embedded Cores Based System-on-Chip
John Sunwoo, Jonathan Harris
VLSI-TESTING, Spring/2004

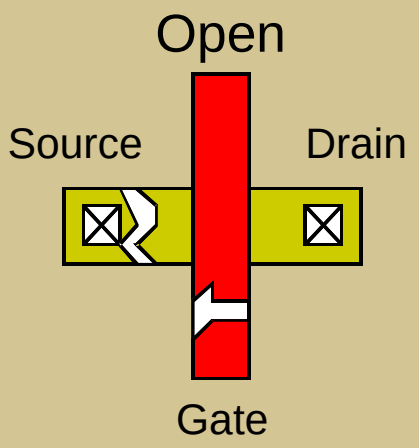
Defect, fault modeling and test metrics

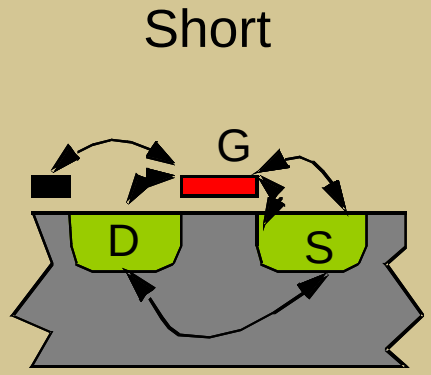
Fault models

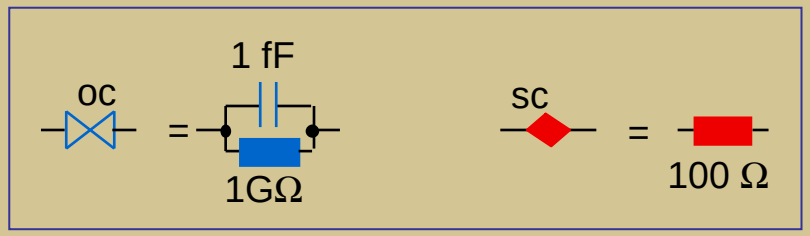
Catastrophic





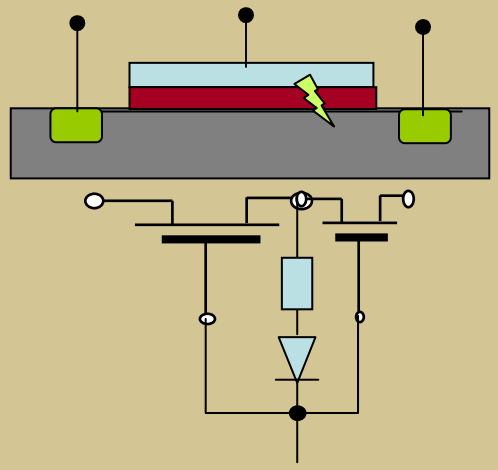


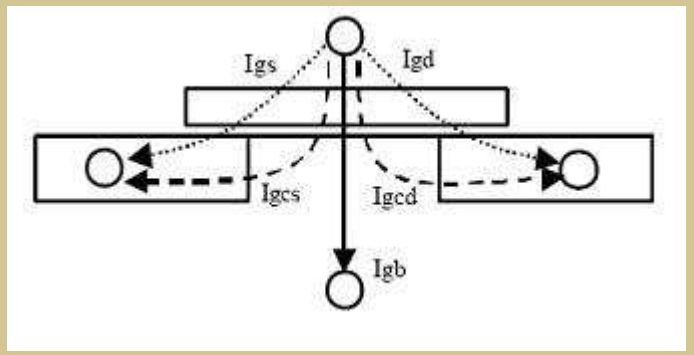




Defect, fault modeling and test metrics

- Gate Oxide Shorts





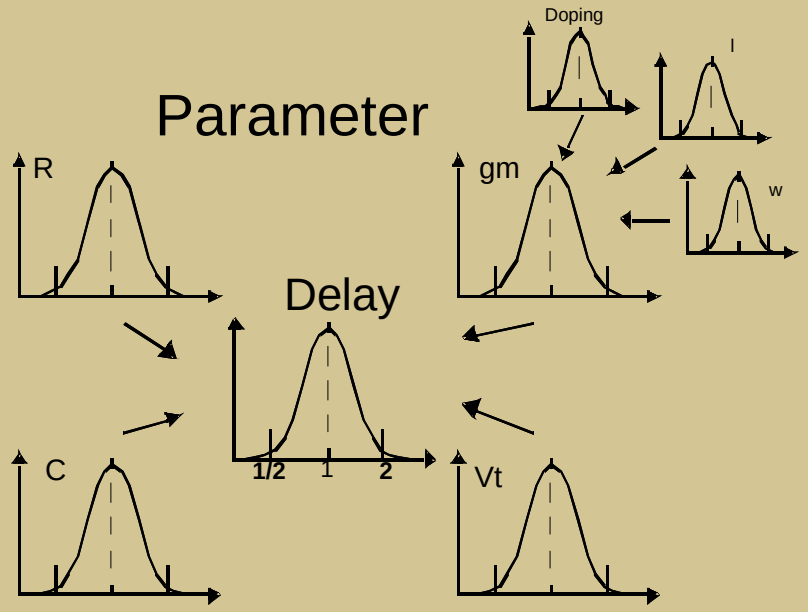
Defect, fault modeling and test metrics

Fault models

Parametric

Parametric faults are simulated by affecting components' parameters (passive and active) with deviations of their nominal values.

E.g. ±5% to ±20% in the values of L, C, R and in the aspect ratio, VTO, KP, of MOS transistors.



Defect, fault modeling and test metrics

Defect Level

- The ultimate objective is to minimize the number of defective parts reaching the market.
  - Ideal value: 0 ppm
  - Typical : < 100ppm

$$DL = 1 - Y^{(1-FC)}$$

- This equation provides an estimation of the defect level as a function of the production yield (Y) and testing fault coverage (FC). Faults are considered equiprobable.

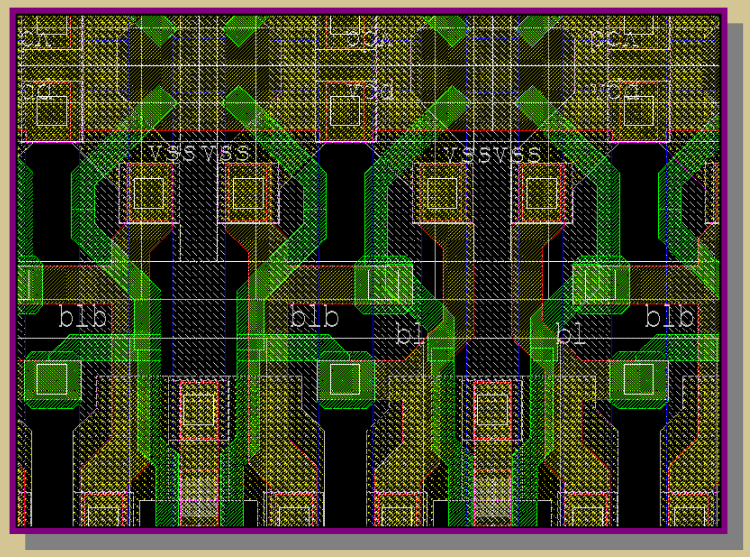
Defect, fault modeling and test metrics

Inductive fault analysis

Considering non equally probable faults, ž introduces a weighted measure of fault coverage.

Each fault weighted by a factor $w_j=-\ln(1-p_j)$ which reflects its occurrence probability

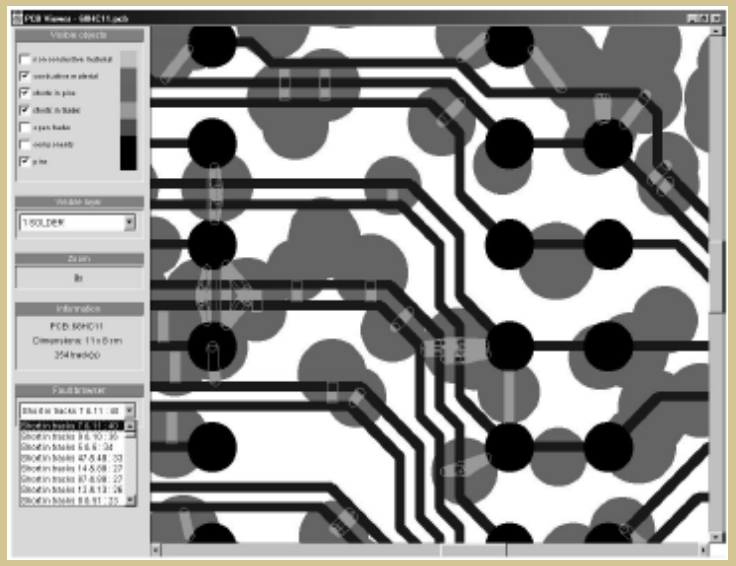
$$DL = 1 - Y^{(1-\check{z})}$$



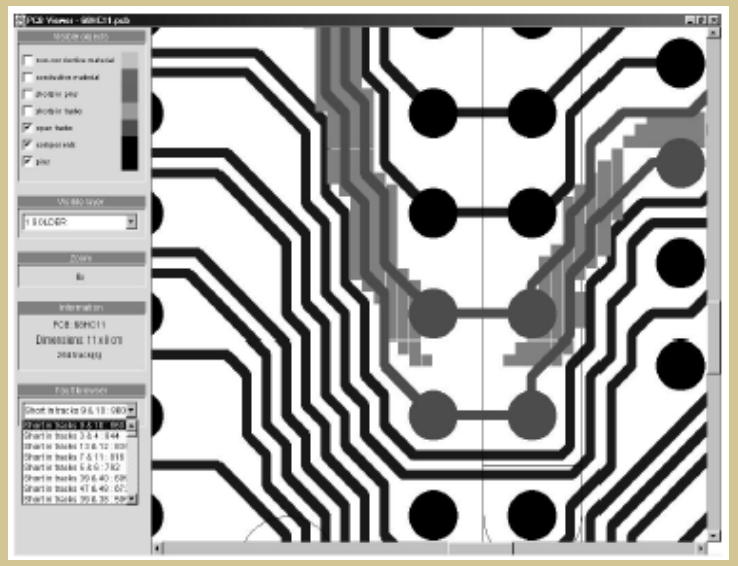
J.T. Sousa, F.M. Gonçalves, J.P.Teixeira, T.W. Williams "Fault Modeling and Defect Projections in Digital ICs" Proceedings of the International Test Conference, 1994.

Defect, fault modeling and test metrics

Extraction of realistic faults and Inductive fault analysis



Extraction of shorts in tracks.

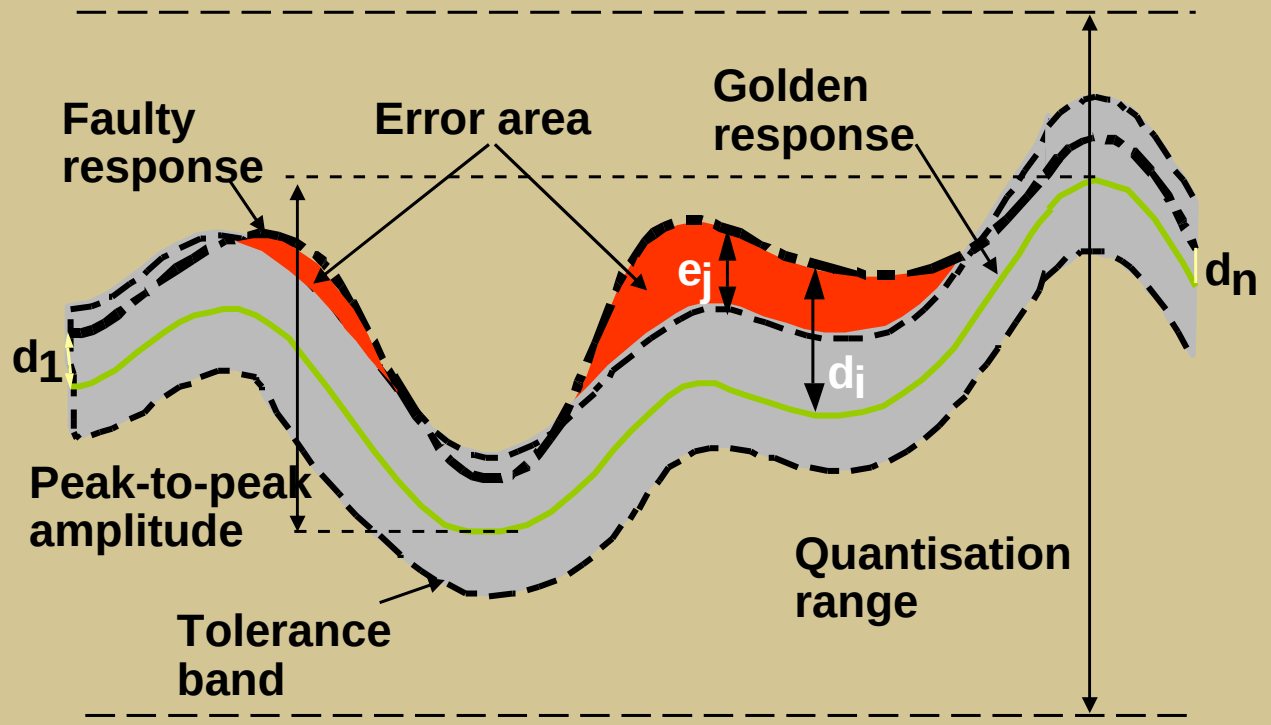


Critical area for shorts in two specified tracks.

"A Tool for Fault Extraction in PCBs",
L.C. Laranjeira, J.Machado da Silva, J.S. Matos
IEEE European Test Workshop 2000

Defect, fault modeling and test metrics

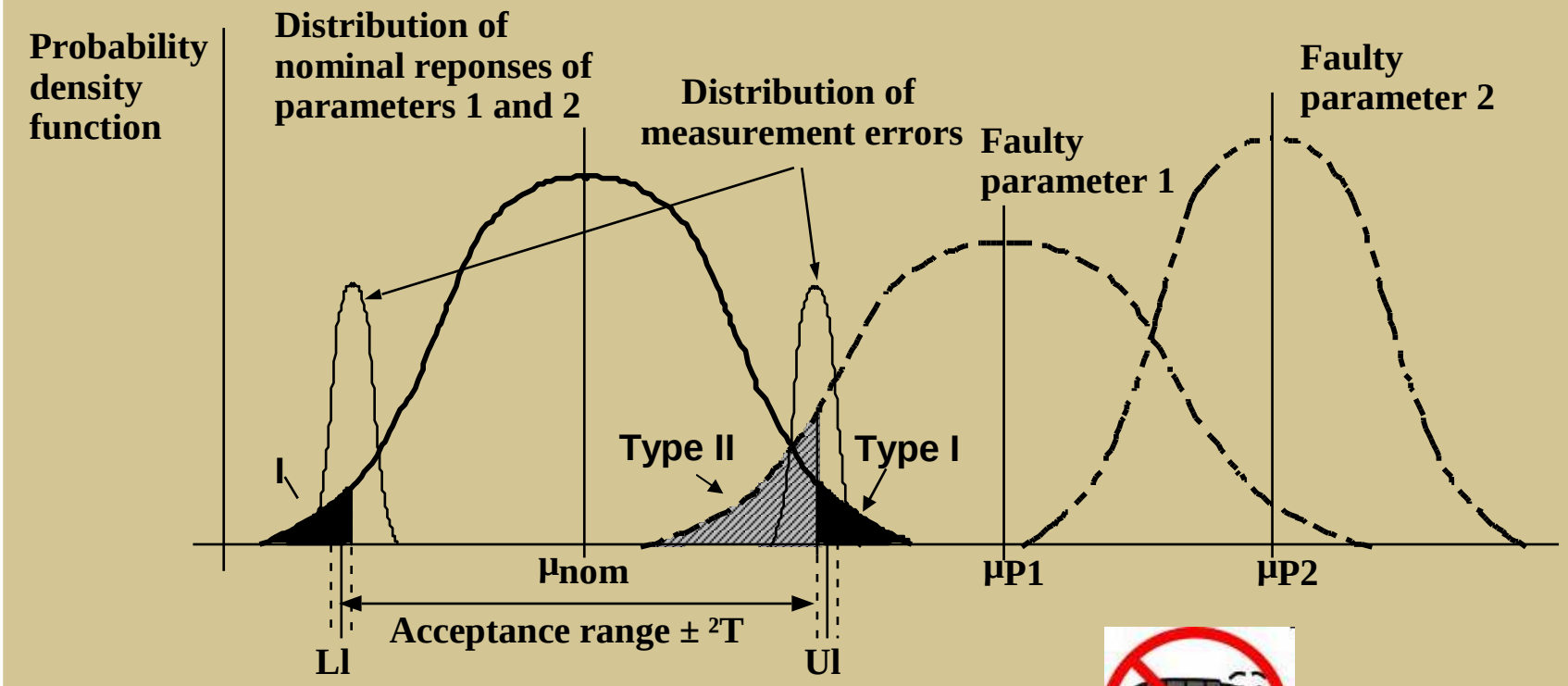
When is a deviation considered a fault?
When is a fault considered detectable?



Signature analysis in amplitude and time domains

Defect, fault modeling and test metrics

Test errors



The cost of validation escapes are enormous
(the Pentium FPDIV bug cost Intel $475 million)

Defect, fault modeling and test metrics

Undetectable fault - no test exists for that fault

Redundant fault - undetectable fault but whose occurrence does not affect circuit operation

Testability = (#detectable faults) / #faults

Effective faults = faults - redundant faults

(These are the ones we must detect if we want to completely test the chip. Since redundant faults cause no harm, they should not be counted against us.)

$$FC = \frac{DetectableFaults}{DefectiveFaults} = 1 - \frac{\int\int_{AB} f_{MT}(m,t)dsdt - P_{PassTest}}{1 - P_{CircuitGood}}$$

(This is a better measure of how well a circuit is tested by a specific test method.)

DfT and BIST

Design for Testability and Built-in Self-Test

IC manufacturers have demanded high performance Automatic Test Equipment

Costly:

- 1 million $

Memory:

- Very high amount of data. Represents 40% of improvements in testers

Mixed-Signal Instrumentation:

- Higher bandwidth, higher sampling rates, higher accuracy, lower noise, etc.
- RF and audio circuits a major challenge, more when noisy digital circuitry is also present.

DUT to ATE interface:

- Higher pin-counts, high frequency & performance probes and sockets.
- No degradation of tester accuracy and noise.

DfT and BIST

Design for Testability and Built-in Self-Test

Design for Testability

Set of techniques/methodologies aiming to improving the capability of generating, applying, and evaluating tests in order to complain with the required fault coverage objectives, subject to time and cost restrictions.

Key concepts:

- Accessibility
- Controllability - capability to activate internal nodes
- Observability - capability to observe internal nodes
- Partitioning

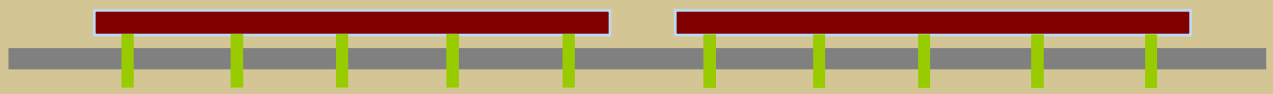
DfT and BIST

Design for Testability and Built-in Self-Test

Test difficulties – accessibility, observability

Plated through hole technology, 200 pin PGA

5 cm



Surface mount technology, 200 pin QFP

3 cm

Multichip module, 200 pad Bare Die

1 cm

DfT and BIST

Design for Testability and Built-in Self-Test

Subtle Forms of DfT

- Robust Circuits
  - Tighter statistical distributions centered between upper and lower test limits.
  - Robust circuits are much less expensive to test
- Design Margin
  - Generous design margins allow devices to be tested on less expensive testers
  - Doubling design margin reduces measurement sampling time by a factor of four
  - Designers often make margin decisions based purely on silicon area without consideration of test impact

DfT and BIST

Design for Testability and Built-in Self-Test

Subtle Forms of DfT

- Avoiding over-specification
  - Question the need for too tight specifications
- Predictability of failure mechanisms
  - Use circuits with simple, “predictable” failure modes even if they require more silicon area
- Tester performance reduction
  - In general, a low frequency tester is much less expensive than a high frequency tester
  - Tester with fewer digital pins is much less expensive

DfT and BIST

Design for Testability and Built-in Self-Test

Advantages of DfT

- Lower test cost
- Ease in test program development
- Higher test efficiency = product and process quality
- DfT observability and controllability provide means for enhanced diagnostic capabilities (throug life-cycle) and processing problems
- Lower cycle time = increased profit
- Test resources available along the whole product life-cycle

DfT and BIST

Design for Testability and Built-in Self-Test

Test auxiliary circuitry

Disadvantages:

- Performance degradation
- Increased power consumption
- Area overhead
- Increased silicon increases development and manufacturing costs
- Increased defect occurrence probability
- Test engineers and design engineers must work as a team to determine the overall cycle time and cost impact of each DfT choice

DfT and BIST

Design for Testability and Built-in Self-Test

Economics of DfT

- Difficult to quantify cost savings
  - Can estimate test cost savings
  - Can't calculate how much cycle time is reduced by a particular DfT choice
  - Lower cycle time results in higher profit margins, but how much higher?
  - How much business would be lost if DfT were not used to improve quality?
- Nevertheless, experience shows that DfT advantages outweigh the disadvantages

DfT and BIST

Design for Testability and Built-in Self-Test

Ad-hoc DfT hints

- Partition the circuit into functionally independent individual blocks
- Choose test nodes with similar electrical characteristics
- Avoid the necessity for multiple test instruments
- Explore as much as possible the resources already available in the circuit
- Choose the test sequence which allows for the best efficiency/test time relationship
- Use as much as simple test schemes as they can be

DfT and BIST

Design for Testability and Built-in Self-Test

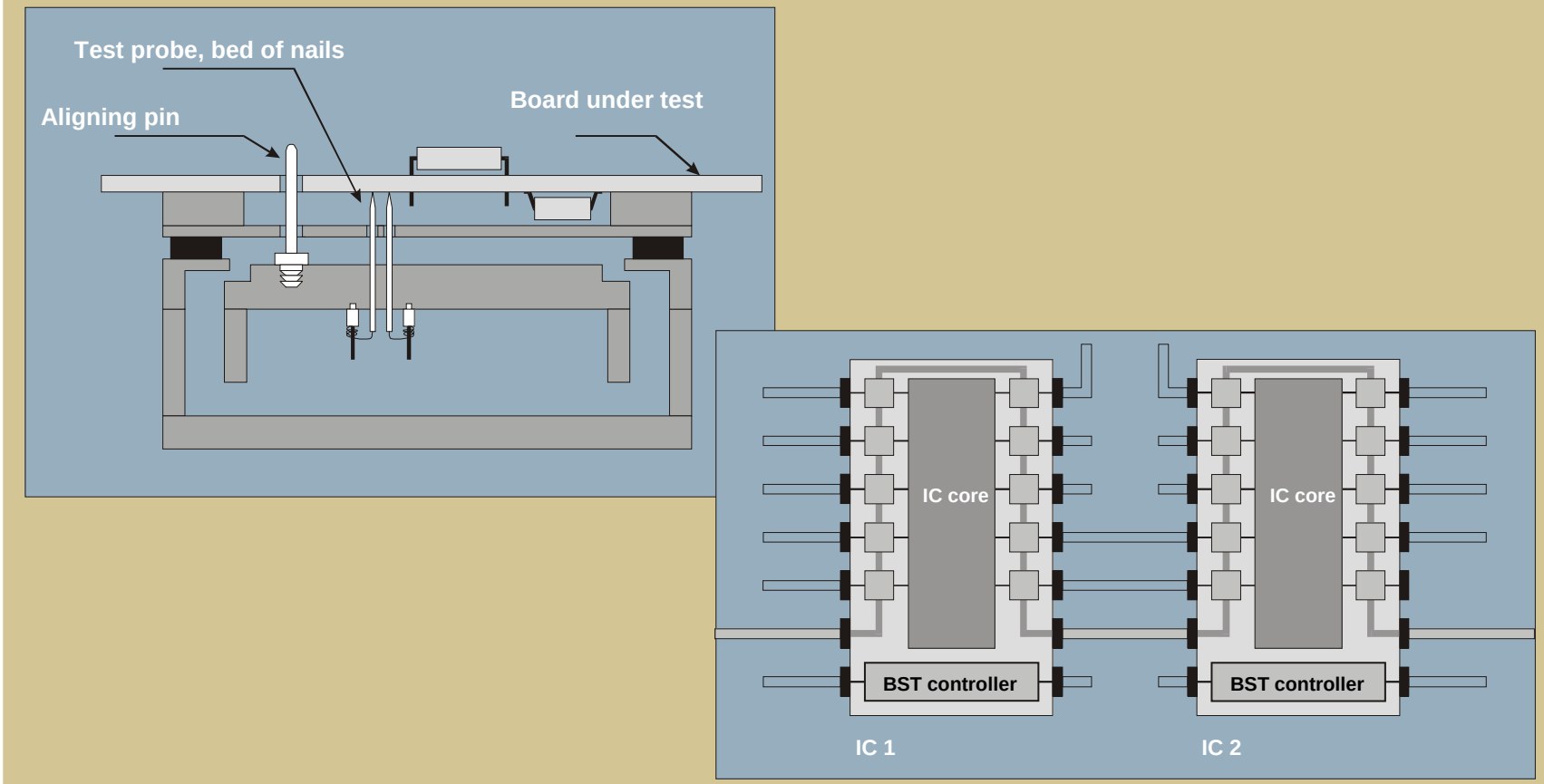
Built-In Self Test (BIST)

- BIST is a subset of DfT
- BIST circuits provide the stimulus and response verification capabilities for testing on-chip
- Allows the DUT to evaluate its own quality with minimum ATE support
- Widely used in digital circuits, but not in analog and mixed-signal circuits

DfT and BIST

Design for Testability and Built-in Self-Test

Accessibility - physical vs. electronic access



DfT and BIST

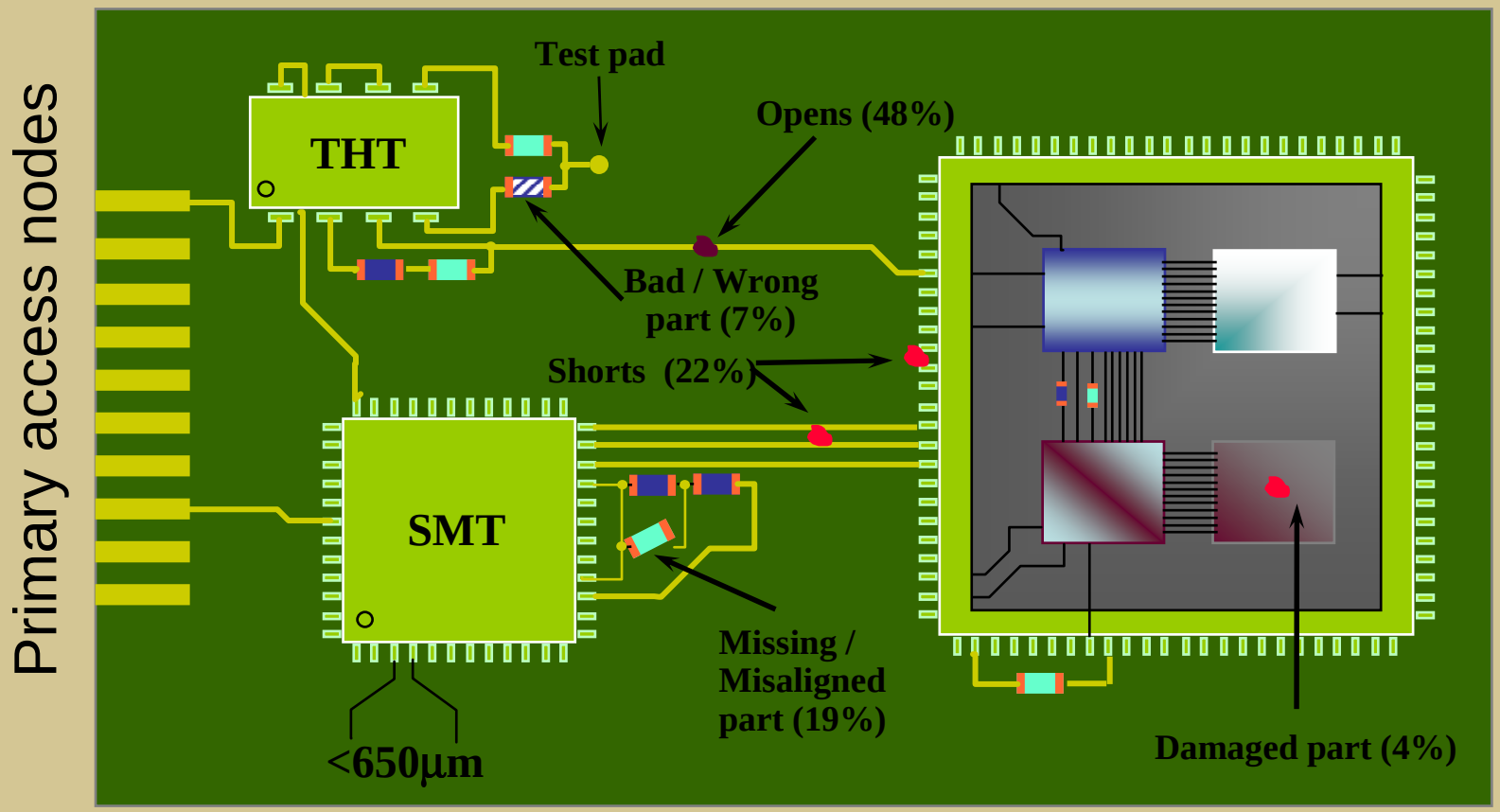
Design for Testability and Built-in Self-Test

The need for hierarchical access

Problems with known good die:

Single chip fault coverage: 95%

MCM yield with 10 chips: $(0.95)^{10} = 60\%$

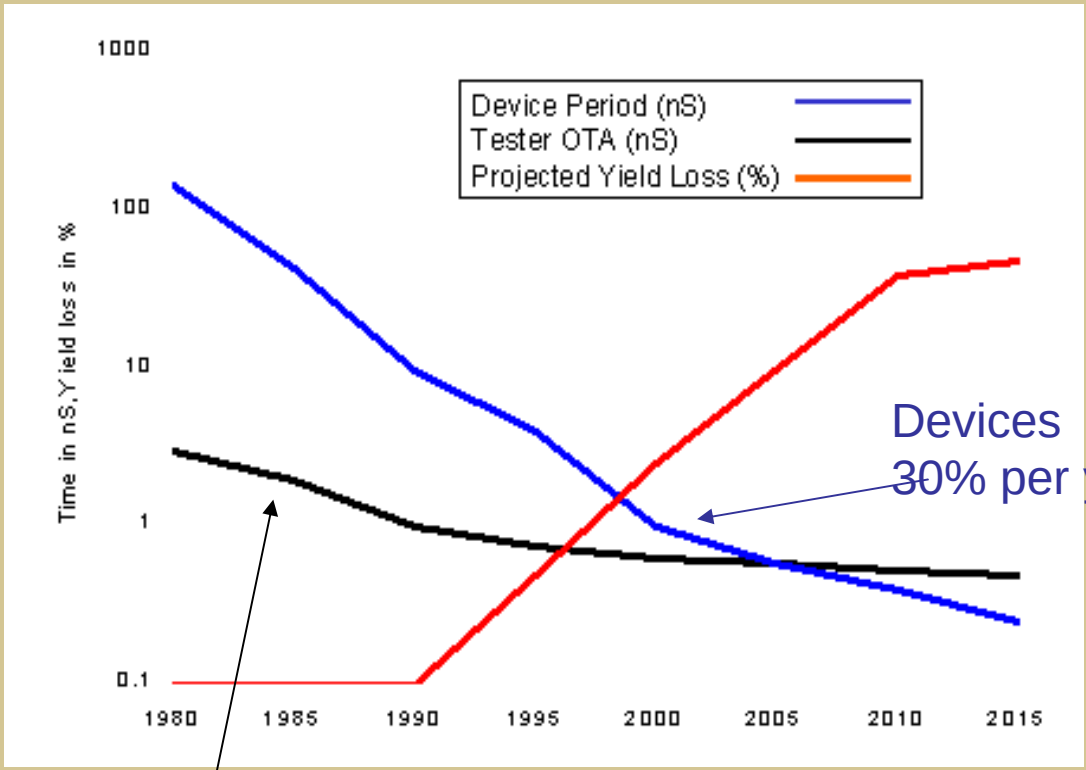


DfT and BIST

Design for Testability and Built-in Self-Test

Tester timing errors

Source: SIA Roadmap



Bandwidth gap between ATE and on-chip signals!

Devices 30% per year

ATE: +12% per year aprox.

DfT and BIST

Design for Testability and Built-in Self-Test

Analogue testing difficulties

- Different functional characteristics of the various blocks embedded in a circuit
- Diversity of amplitude and time characteristics of the different signals present in the same circuit
- Higher volume and accuracy of data to be processed
- Test methods and instruments are often inadequate to test the new circuit's functionalities
- Lack of fast and generic tools to develop and evaluate test methods (test generation, simulation, stimuli generation)
- Higher sensitivity to process variations and measurement inaccuracy

DfT and BIST

Design for Testability and Built-in Self-Test

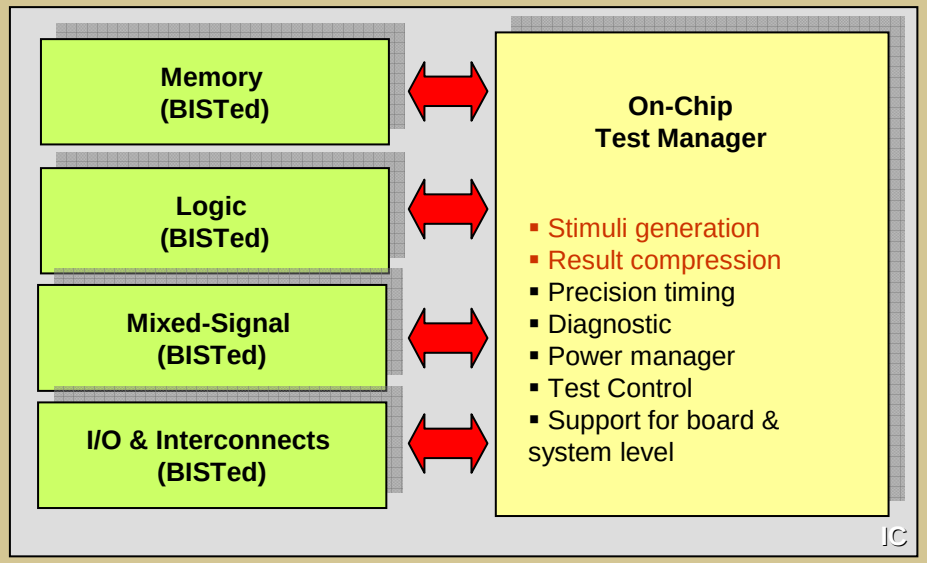
- There is no other way to cope with the cost and complexity of future ICs.
- Do not try to emulate a complete external testing - this is not practical in most cases. Functional testing must be reduced.
- Reduce costly or non-practical on-chip tests
  - Structural test is a clear powerful complement to functional testing
  - Structural test related to the I/O functional behavior
- Accessing: Yes, but non-intrusive

DfT and BIST

Design for Testability and Built-in Self-Test

The BIST Solution

- On-chip resources can run at the same speed than the CUT
- Avoid the need of external accessing
- Reduce interface to low bandwidth (control, low freq. signals, etc.)
- Customized test



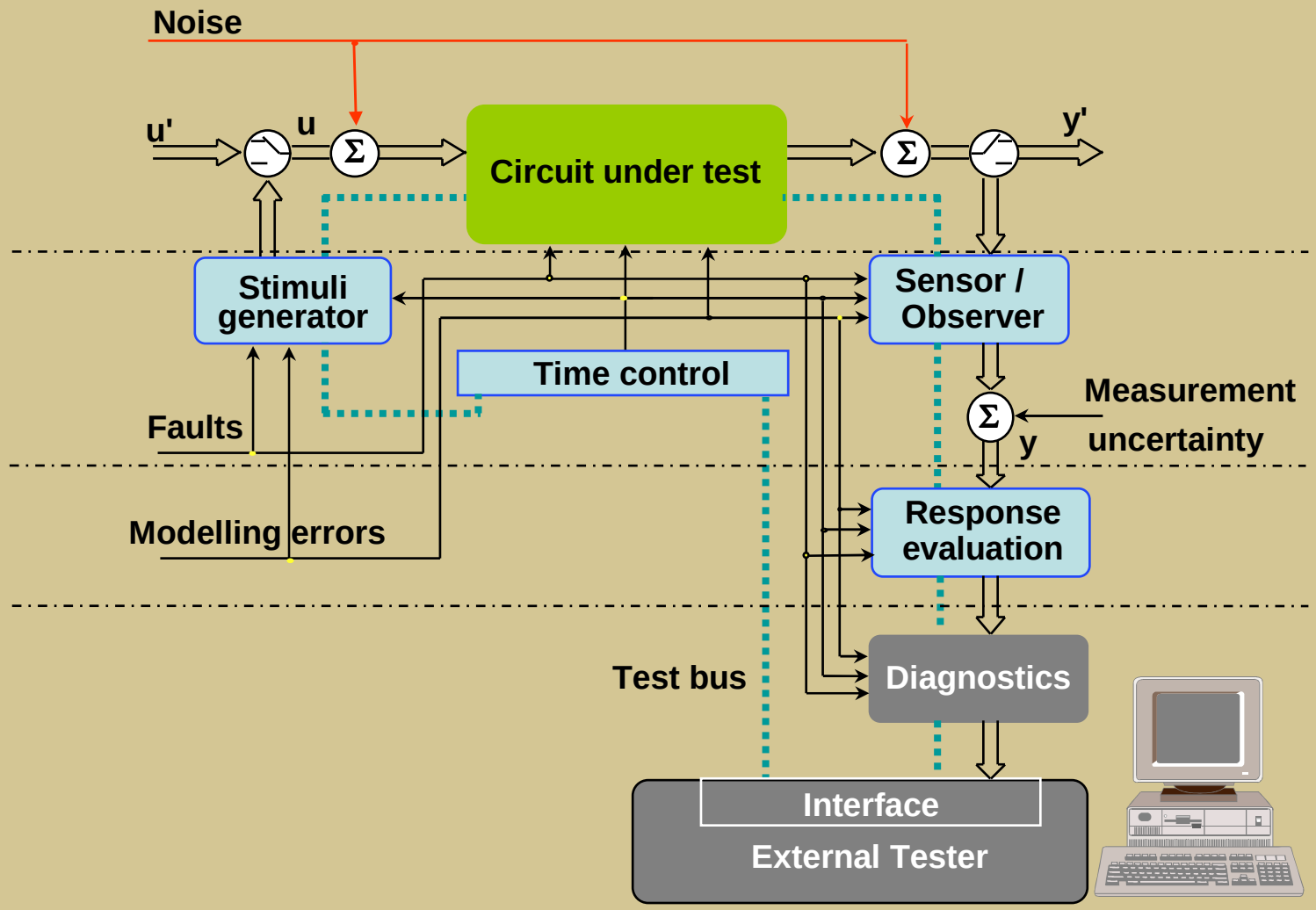
DfT and BIST

Design for Testability and Built-in Self-Test

Key aspects

- Re-usable and structured DfT & BIST techniques
  - » Reduce I/O data rate requirements,
  - » Enable low pin count testing, and
  - » Reduce the dependence on expensive instruments.
- Structured Test planning
  - » Enable hierarchical testing
  - » Enable the re-use of on-chip resources (DSP, uP, etc.)
  - » Facilitate parallel testing
  - » etc.
- Standardized Test Access Mechanism

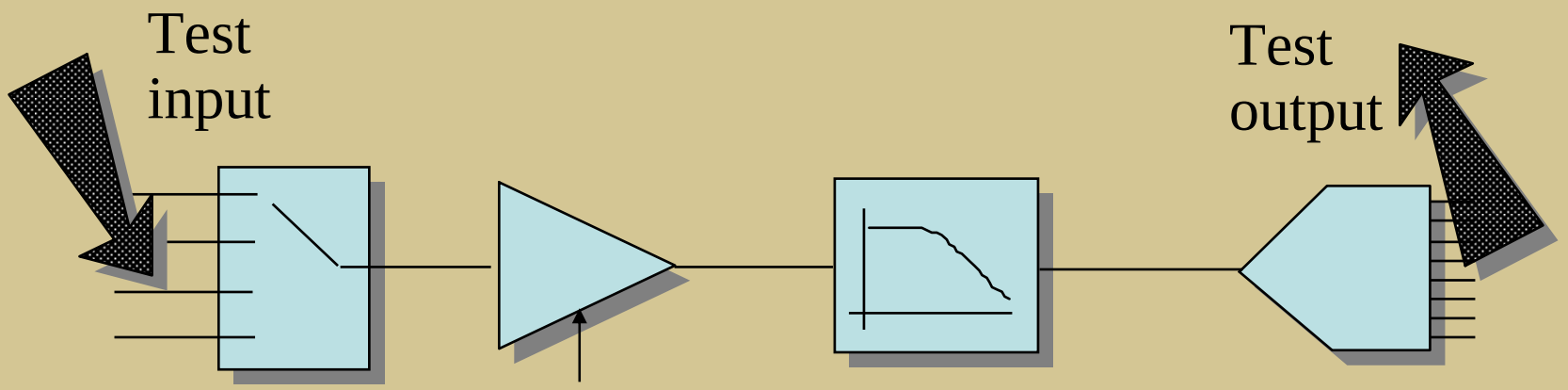
A generic test system model



DfT and BIST

Design for Testability and Built-in Self-Test

- Testing embedded macros - Test what?



Mux	PGA	Filter	ADC
- R_{on}	- Gain	- Gain	- DNL
- R_{off}	- Bandwidth	- Bandwidth	- INL
- V_{br}	- Slew-rate	- Zin	- SINAD
- f_{max}	- THD	- Non-linearity	- N_{ef}

DfT and BIST

Design for Testability and Built-in Self-Test

Approaches

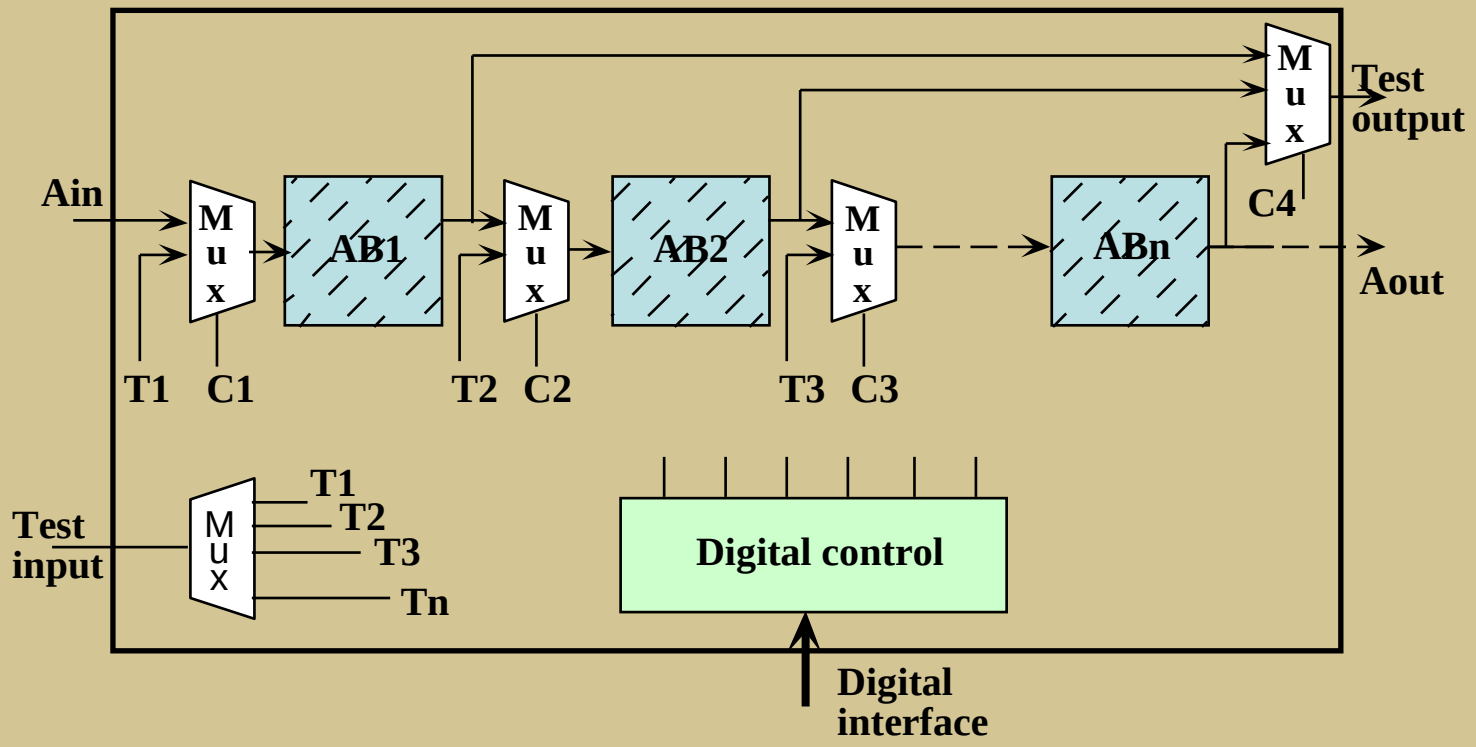
- Infrastructures to access internal test nodes
- Inclusion of observation and evaluation blocks
- Local test stimuli generation
- Functional reconfiguration based schemes
- Built-in self-test

DfT and BIST

Design for Testability and Built-in Self-Test

Infrastructures to access internal test nodes

- Multiplexing test nodes



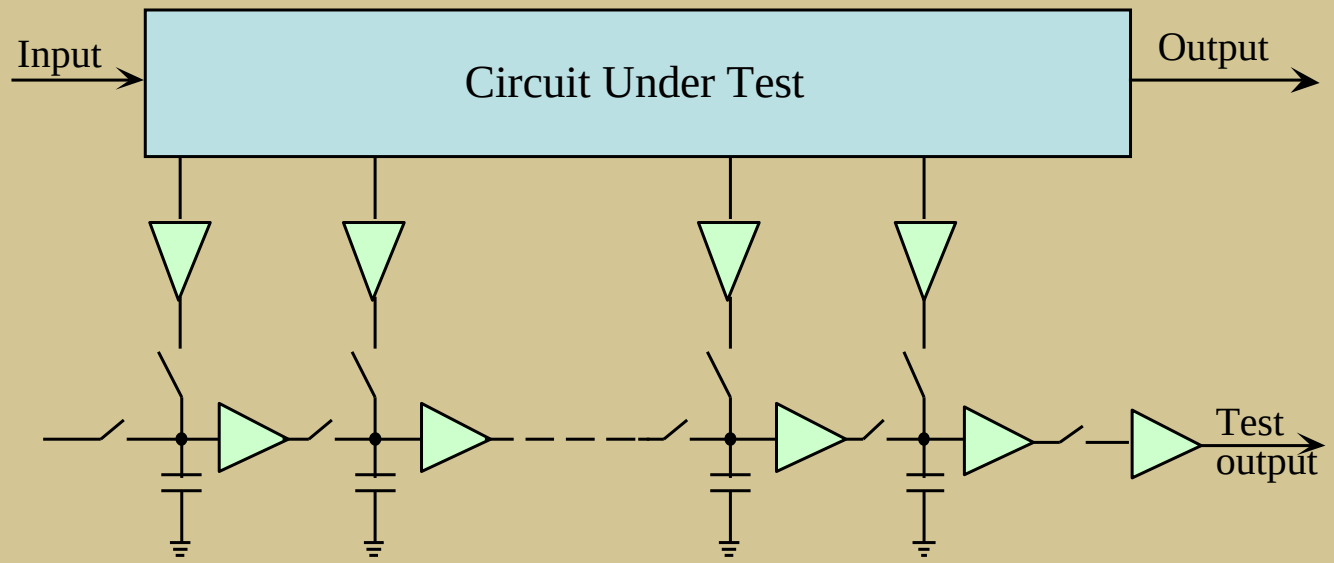
A framework for Design for Testability of Mixed Analog/Digital Circuits
M. Jarwala, IEEE 1991 Custom Integrated Circuits Conference

DfT and BIST

Design for Testability and Built-in Self-Test

Infrastructures to access internal test nodes

- Analogue scan (observation)



Built-in self-test (BIST) structure for analog fault diagnosis
C. L. Wey, IEEE Trans. Instrumentation & Measurement, vol.39, n.3, 1990

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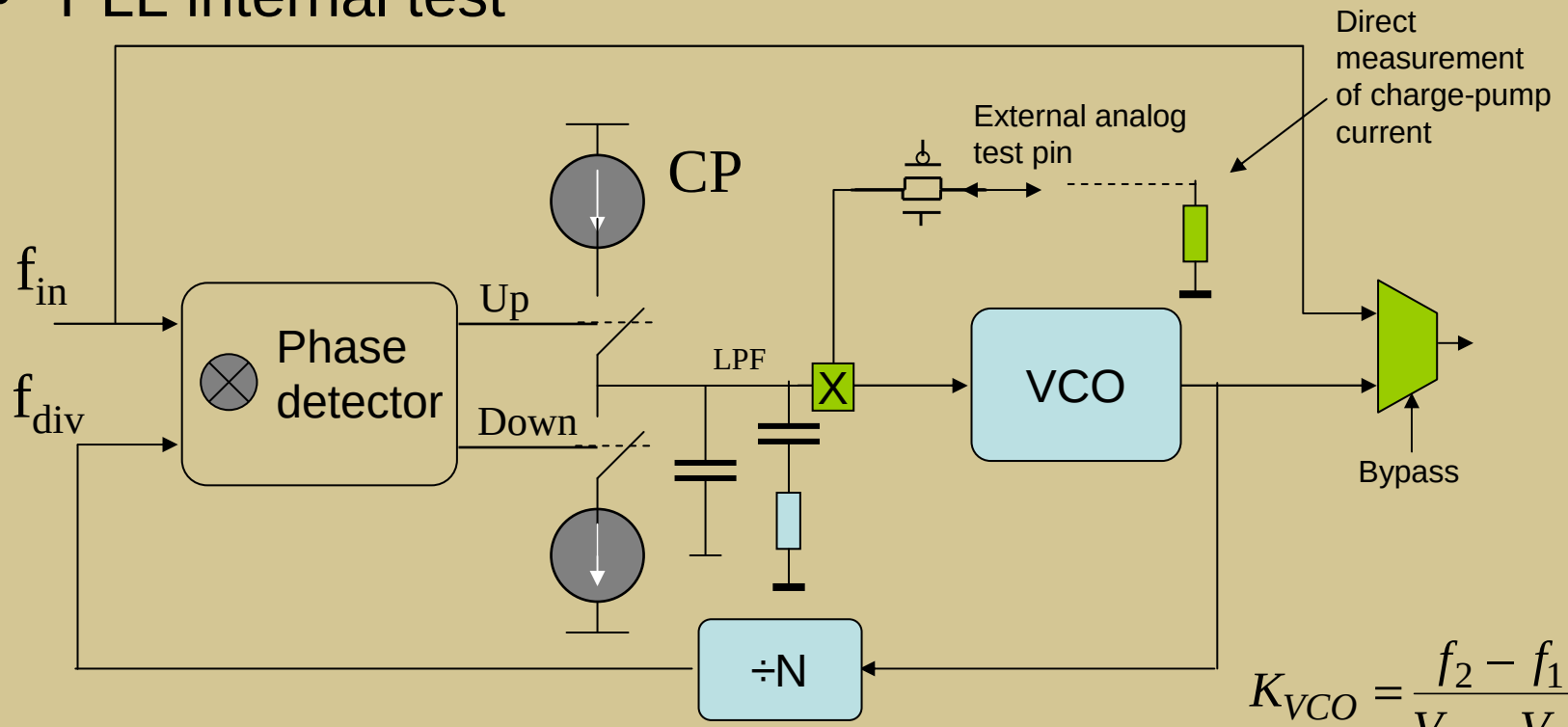
Design for Testability and Built-in Self-Test

Infrastructures to access internal test nodes

- PLL internal test



$$K_{VCO} = \frac{f_2 - f_1}{V_{t2} - V_{t1}}$$

Motivations towards BIST and DfT for embedded charge-pump phase-locked loop frequency Synthesisers. M.J. Burbidge, A. Lechner, G. Bell and A.M.D. Richardson
IEE Proc.-Circuits Devices Syst., Vol. 151, No. 4, August 2004

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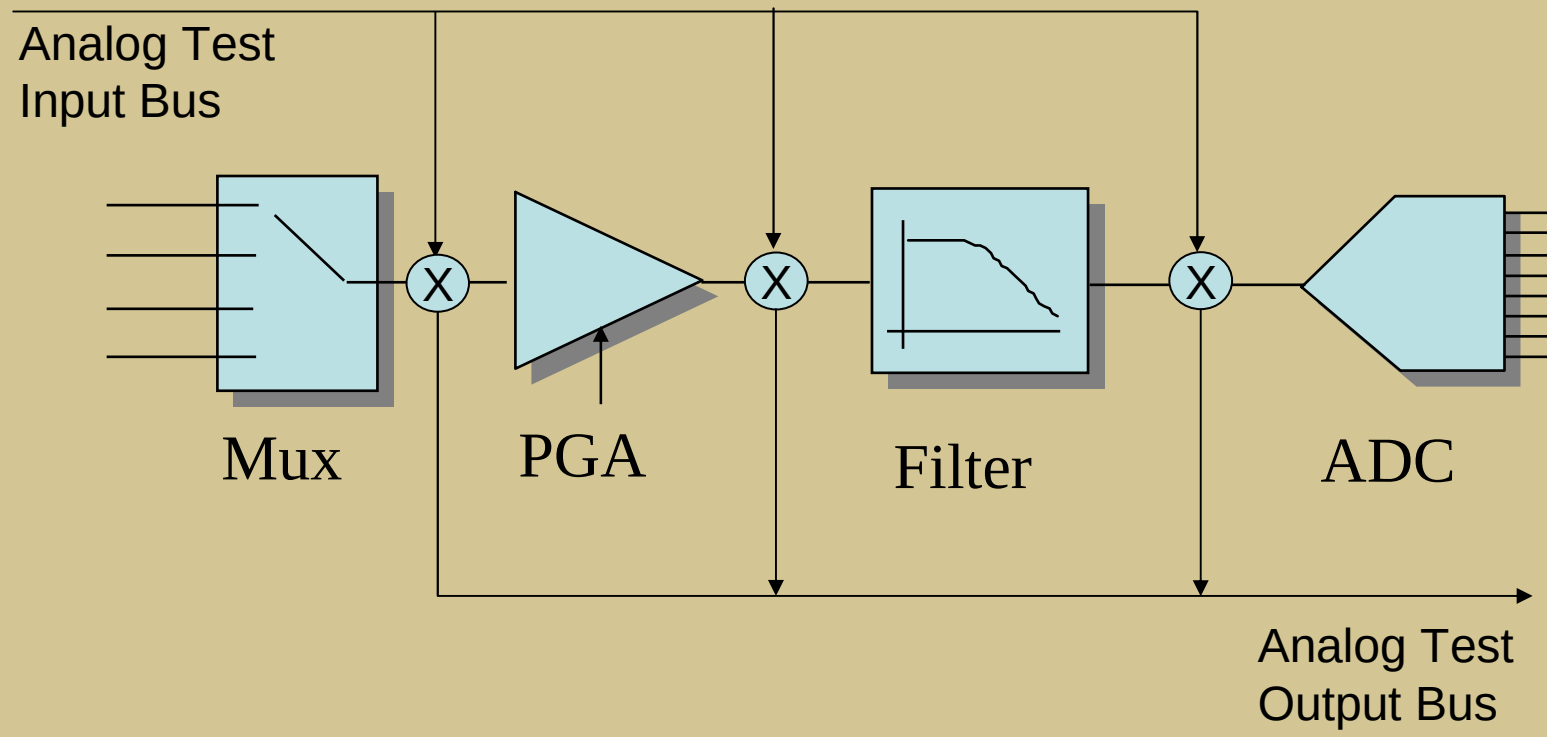
Design for Testability and Built-in Self-Test

Infrastructures to access internal test nodes

- Design Diagnostics



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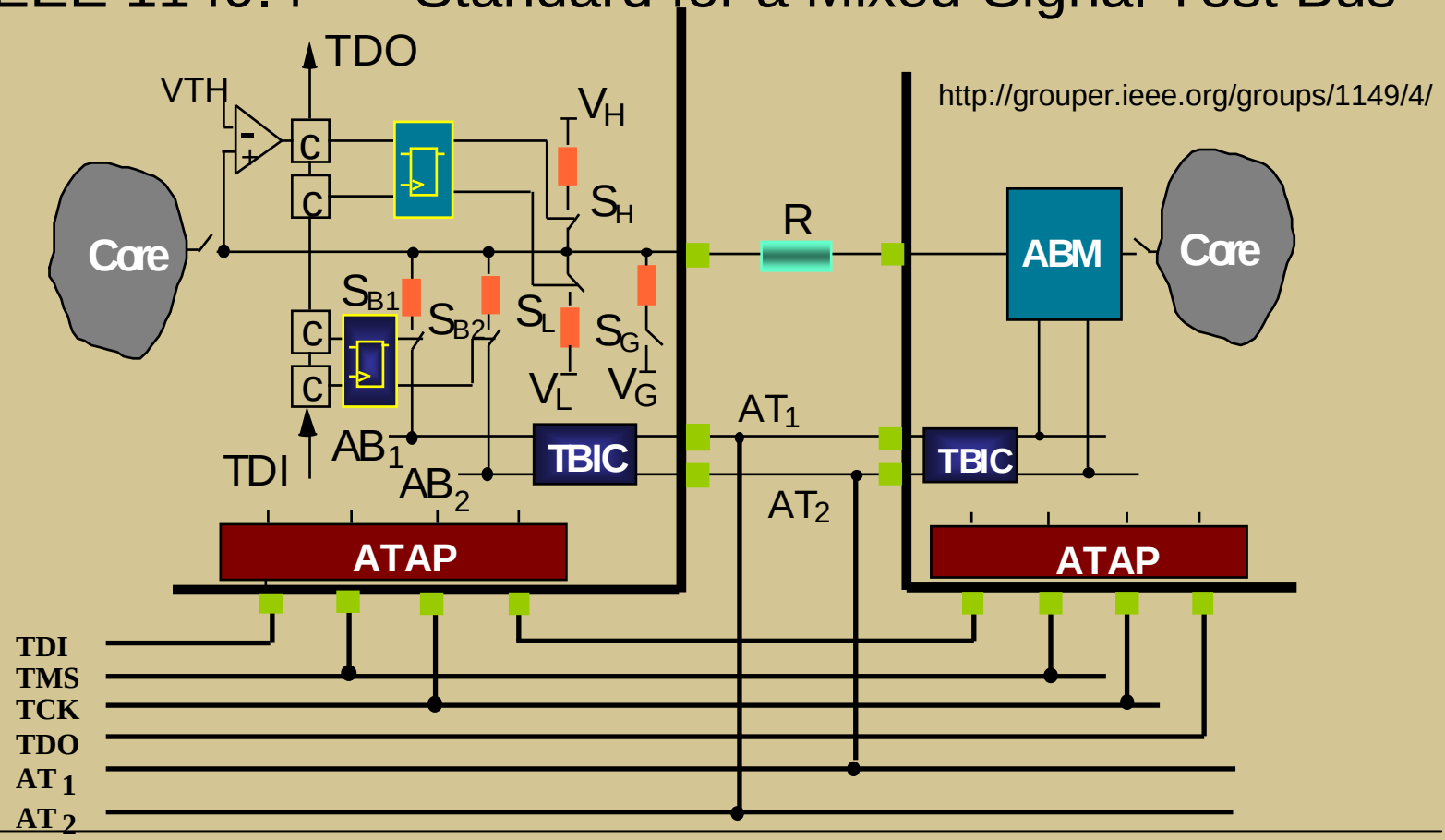
Design for Testability and Built-in Self-Test

Infrastructures to access internal test nodes

- IEEE 1149.4 — Standard for a Mixed-Signal Test Bus



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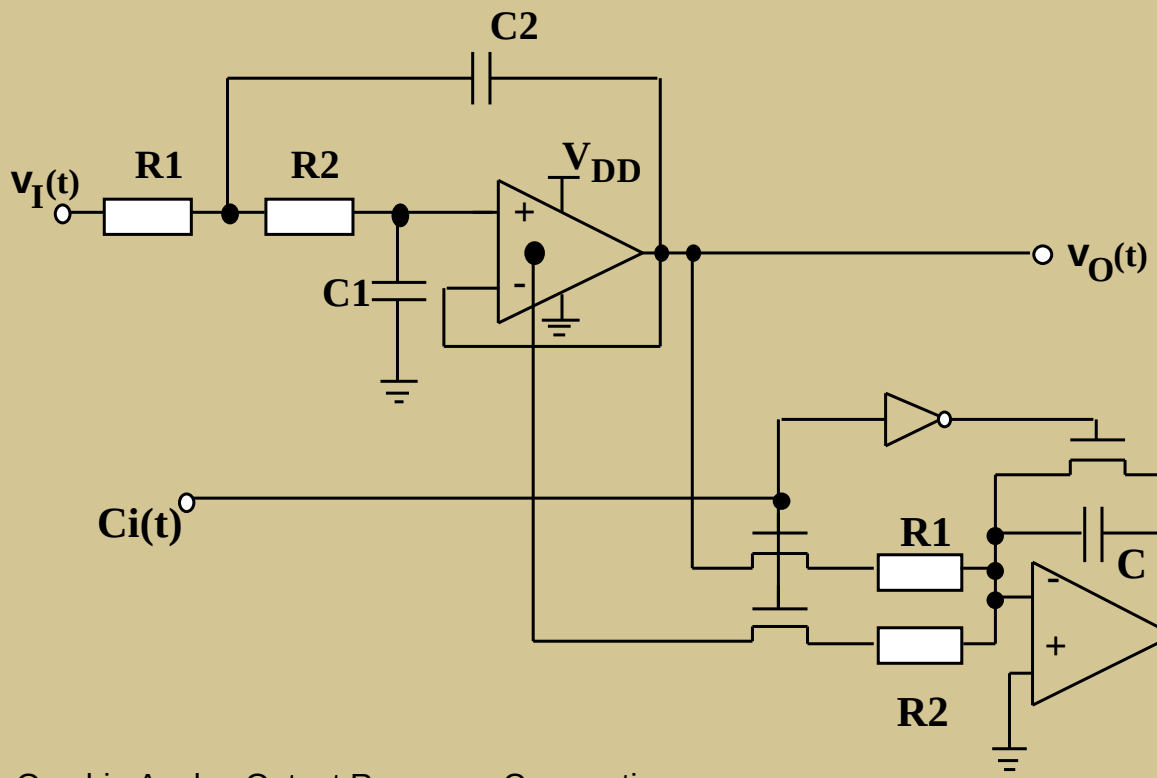
Design for Testability and Built-in Self-Test

Insertion of observation and evaluation blocks



$$S(t) = -\frac{1}{C}\int \sum_{i=1}^{n} \frac{v_i(t)}{R_i} dt$$

On-chip Analog Output Response Compaction
M. Renovell, F. Azais, Y. Bertrand
European Design & Test Conference, 1997

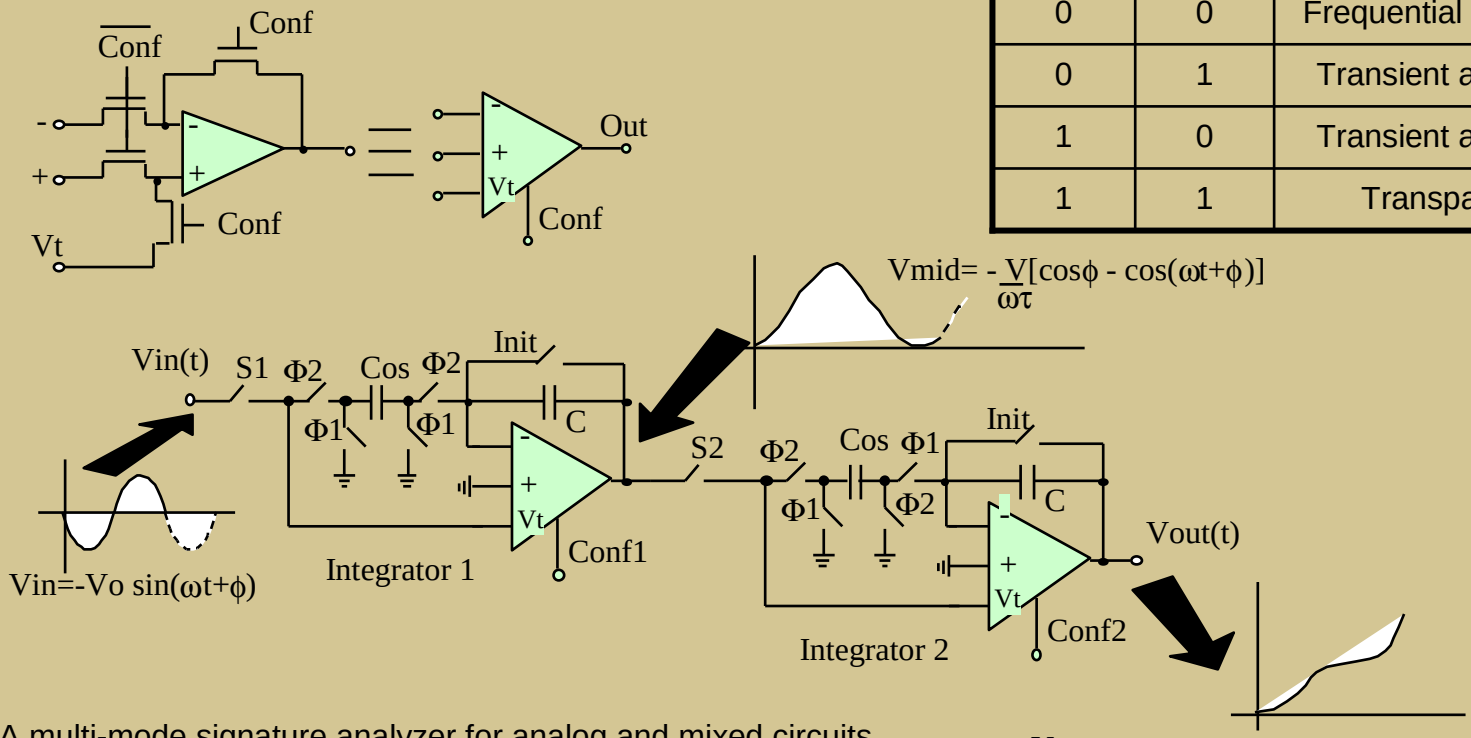
DfT and BIST

Design for Testability and Built-in Self-Test

Insertion of observation and evaluation blocks

- Multi-mode signature analyser

Conf1	Conf2	Mode
0	0	Frequential analyzer
0	1	Transient analyzer
1	0	Transient analyzer
1	1	Transparent



A multi-mode signature analyzer for analog and mixed circuits
M. Renovell, M. Lubaszewski, S. Mir, F. Azais, Y. Bertrand
Proceedings of *International Conference on VLSI,* 1997.

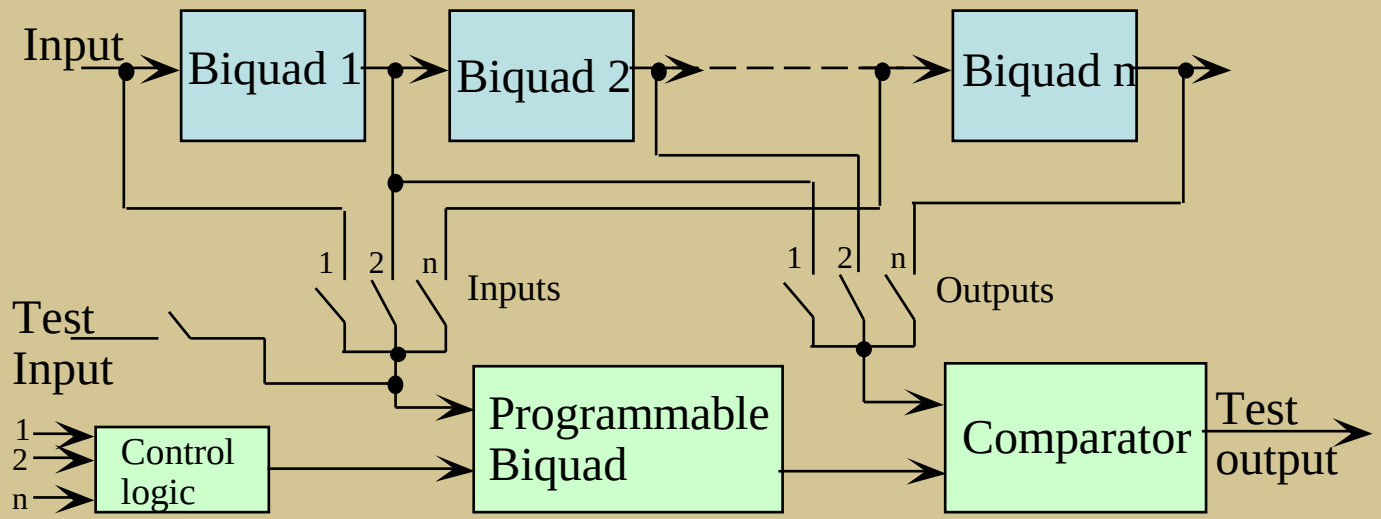
$$Vout = -\frac{V}{(\omega\tau)^2}[-\sin(\omega t+\phi) + \omega t.\cos\phi + \sin\phi]$$

DfT and BIST

Design for Testability and Built-in Self-Test

Insertion of observation and evaluation blocks

- Use of a Programmable Biquad



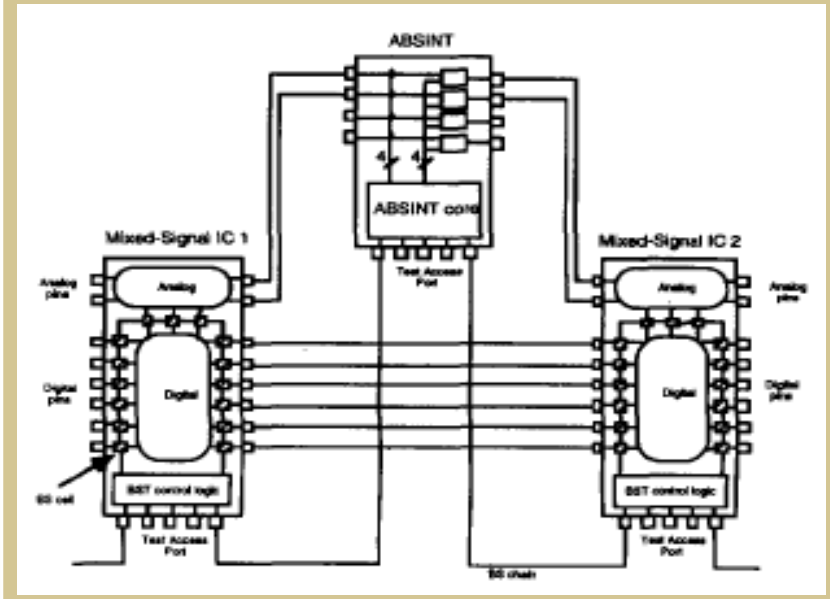
Improving the Testability of Switched-capacitor Filters
J.L.Huertas, A. Rueda, D.Vázquez
Journal of Electronic Testing, November 1993

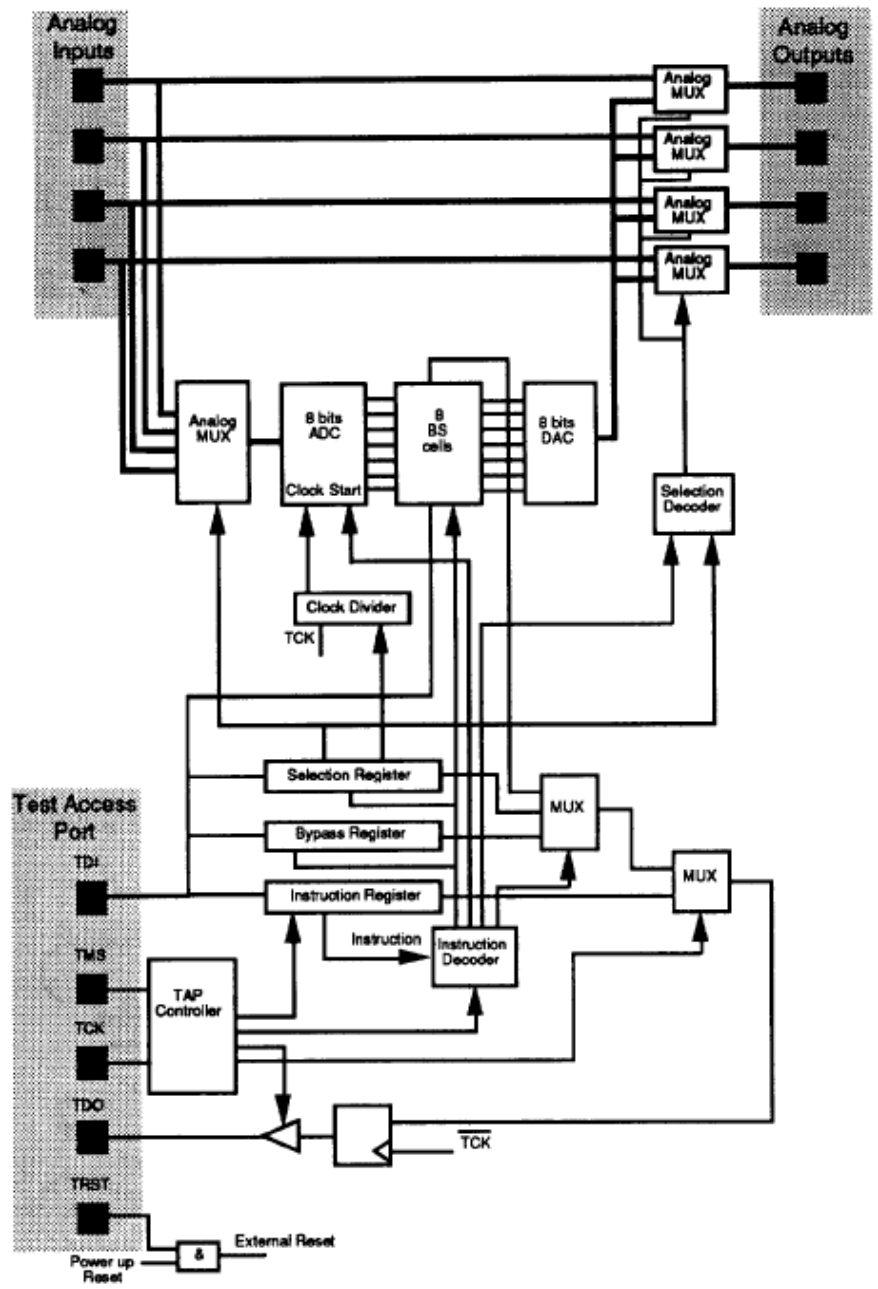
DfT and BIST

Design for Testability and B

Insertion of observation

- ABSINT





"*Control and observation of analog test nodes*", IEEE ITC, 1993

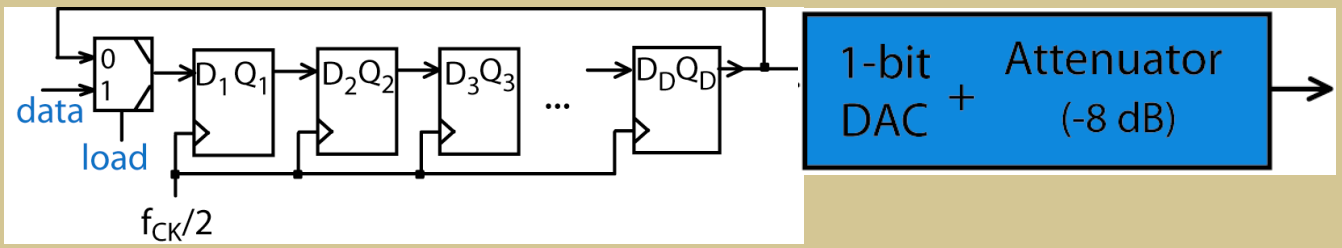
"*An Approach to Testability Improvement of Mixed-Signal Boards*", IEEE ISCAS, 1994

DfT and BIST

Design for Testability and Built-in Self-Test

Local test stimuli generation

- ΣΔ modulated signals



Characteristics

- Bit-Stream obtained from a 3th order ΣΔ Modulator
- 804 bit length
- f_{IN} at 5 kHz
- Clocked at $f_{CK}/2$

A BIST Scheme for SNDR Testing of ΣΔ ADCs Using Sine-Wave Fitting
Luis Rolindez, Salvador Mir, Ahcene Bounceur and Jean-Louis Carbonero
Proceedings of the 24th IEEE VLSI Test Symposium (VTS'06)

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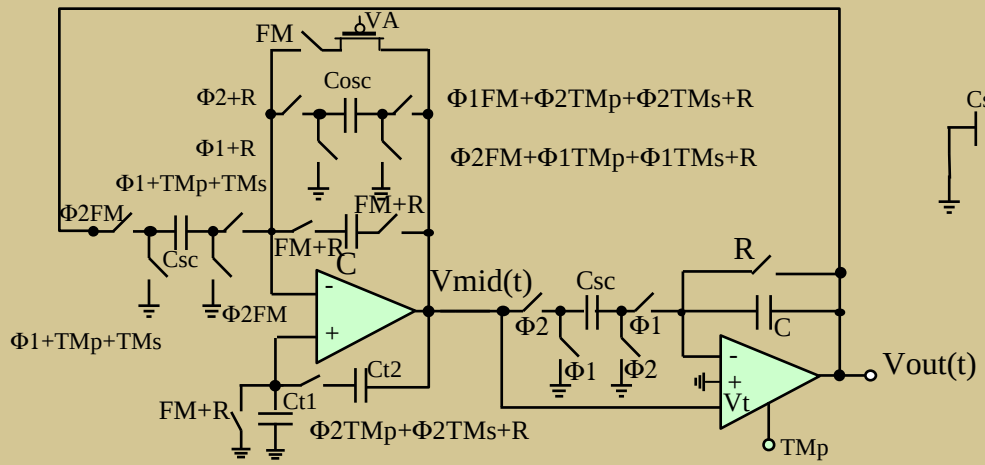
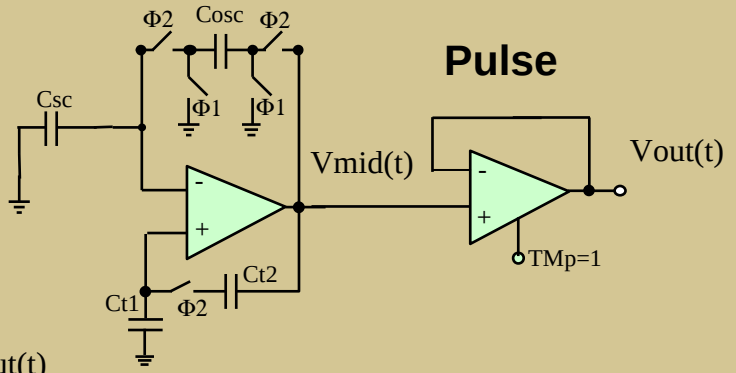
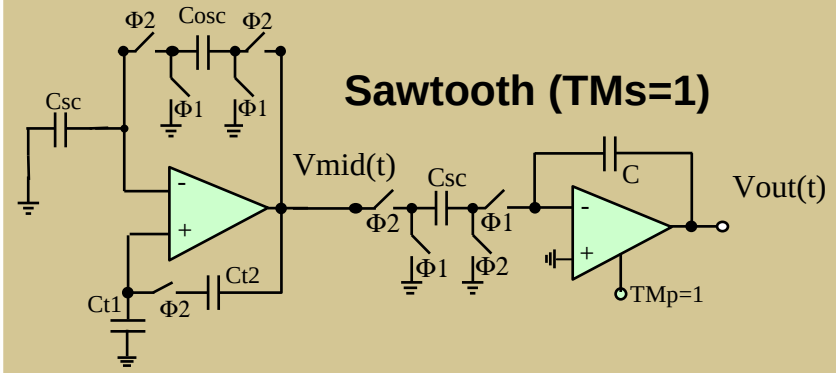
Design for Testability and Built-in Self-Test

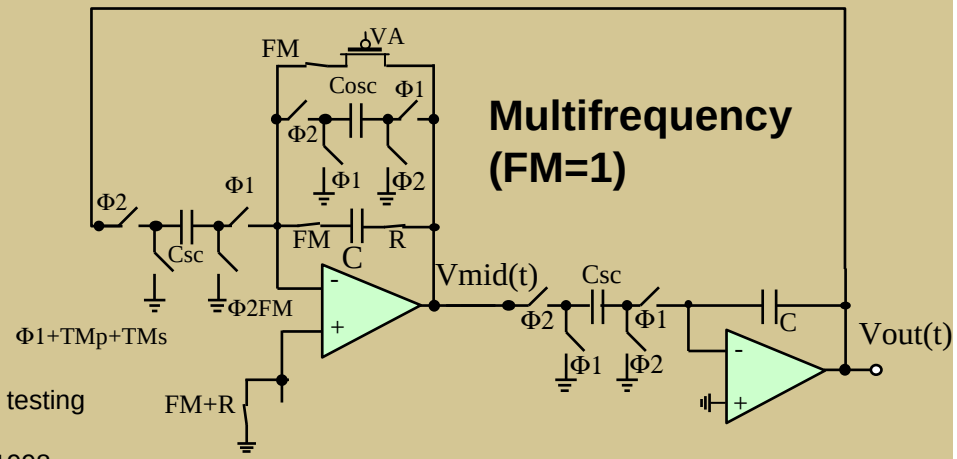
Local test stimuli generation

- Multi-mode stimuli generator









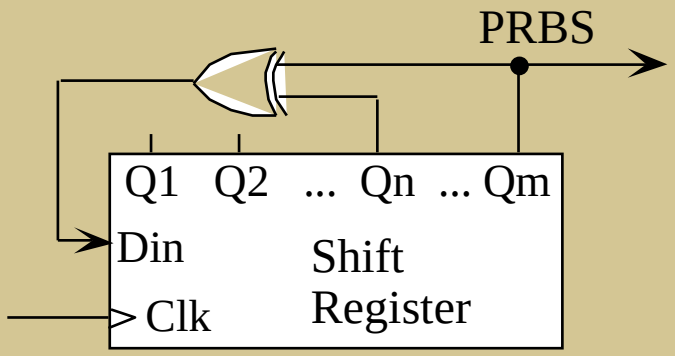
A built-in multi-mode stimuli generator for analogue andmixed-signal testing
Lubaszewski M., Renovell M. Mir, S. Azans, F. Bertrand, Y.
Integrated Circuit Design, Proceedings. XI Brazilian Symposium on 1998

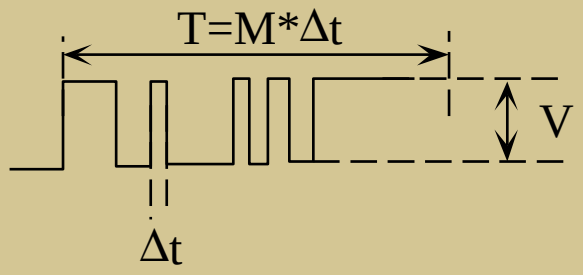
DfT and BIST

Design for Testability and Built-in Self-Test

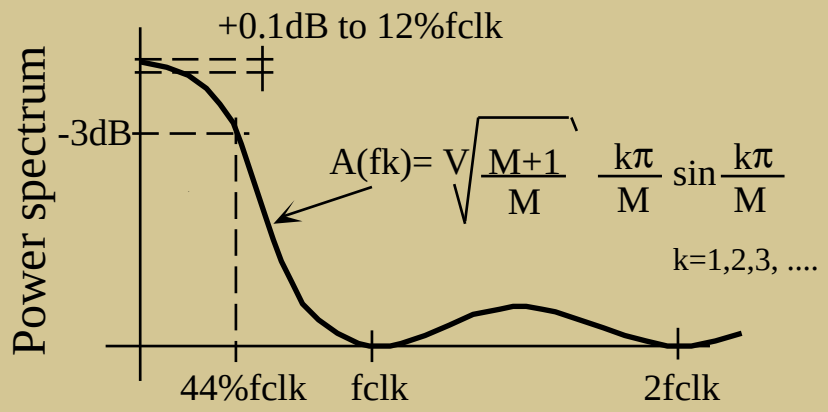
Local test stimuli generation

- Generation of pseudo-random signals





m	n	length (2^m-1)
4	3	15
6	5	63
8	(4,5,6)	255
10	7	1023
15	14	32767



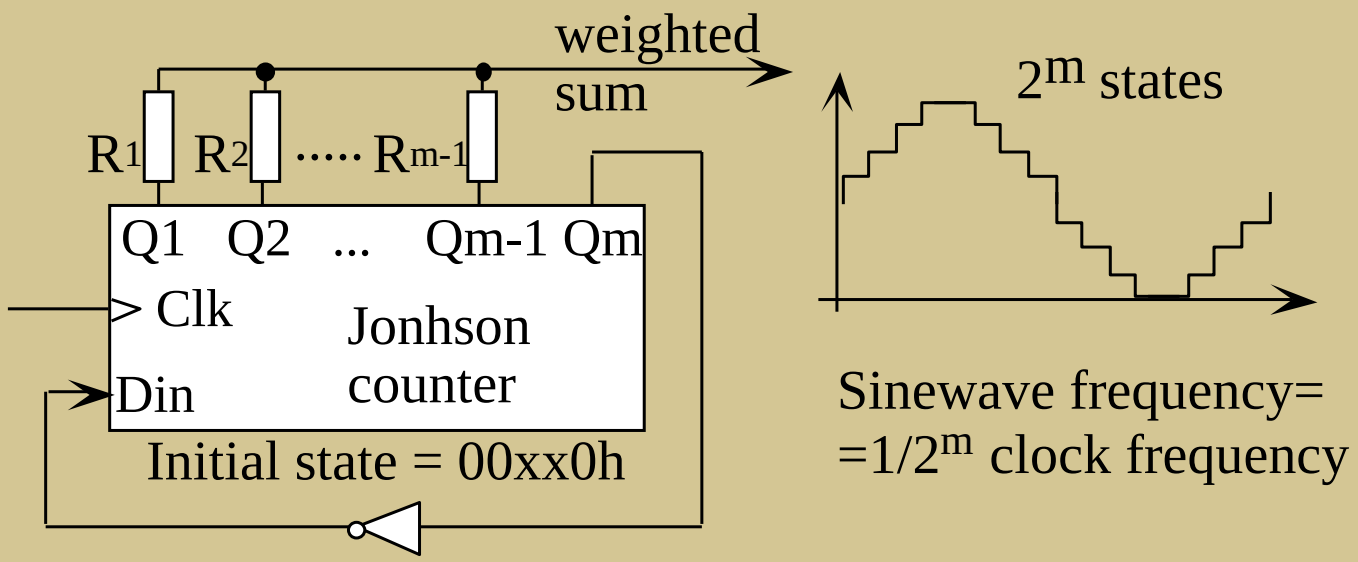
$f_k = k/(M\Delta t)$

DfT and BIST

Design for Testability and Built-in Self-Test

Local test stimuli generation

- Discrete sinewave generation

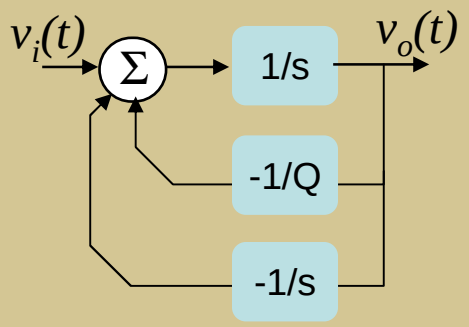


For correctly weighted resistors
the 1st harmonic is of order 2^m-1

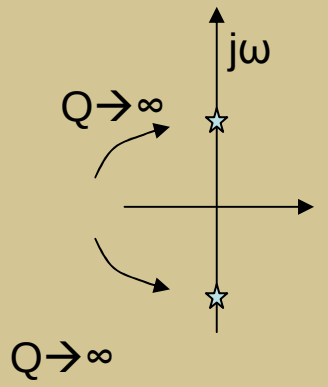
DfT and BIST

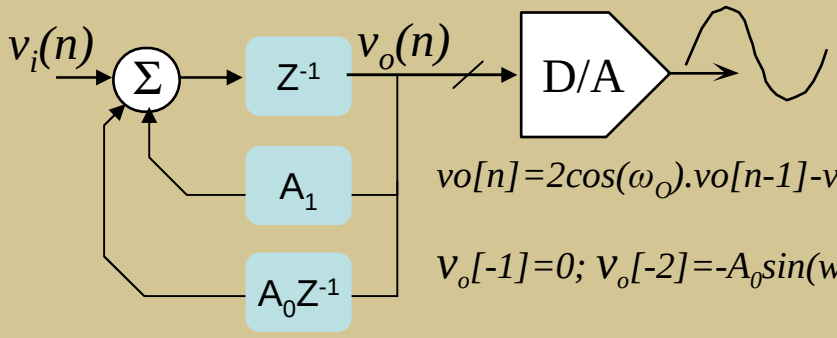
Design for Testability and Built-in Self-Test

- Sinewave oscillator



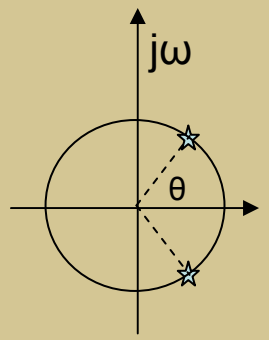
$$\frac{v_o(t)}{v_i(t)} = \frac{s}{s^2 + s/Q + 1}$$





$vo[n] = 2\cos(\omega_O).vo[n-1] - vo[n-2]$

$v_o[-1] = 0;\ v_o[-2] = -A_0 \sin(w_O);\ w_O = 2\pi f_O / f_S$



$$\frac{V_o(z)}{V_i(z)} = \frac{z^{-1}}{1 - A_1 z^{-1} - A_0 z^{-2}}$$

$$Zp_{1,2} = A_1/2 \pm j\sqrt{-A_1^2 - 4A_0}/2$$

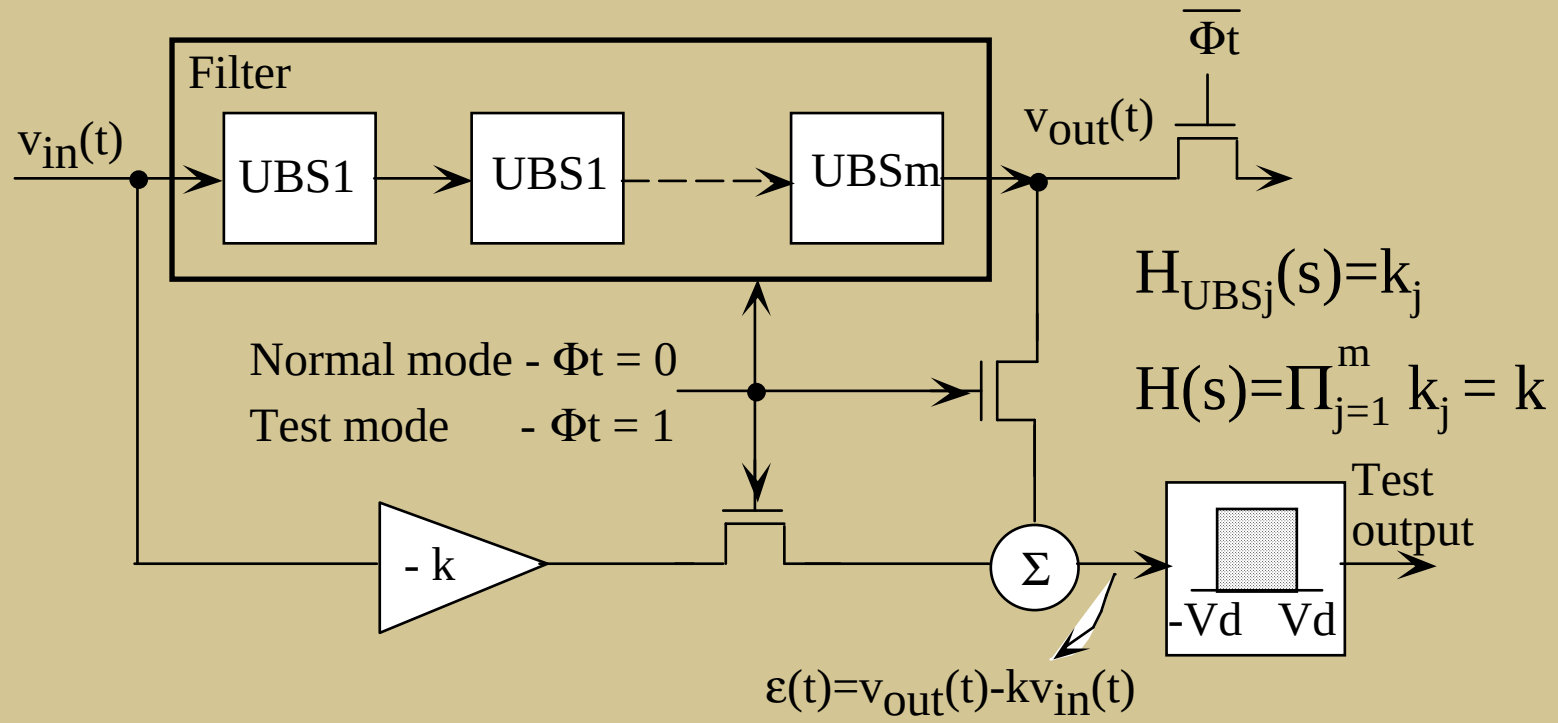
$$Zp_{1,2} = \cos(\omega_0 T_s) \pm j \sin(\omega_0 T_s)$$

DfT and BIST

Design for Testability and Built-in Self-Test

Functional reconfiguration based schemes

- Reconfiguration of universal biquadratic sections



A New Strategy for Testing Analog Filters
D. Vázquez, A. Rueda, J.L. Huertas
12th VLSI test Symposium, 1994

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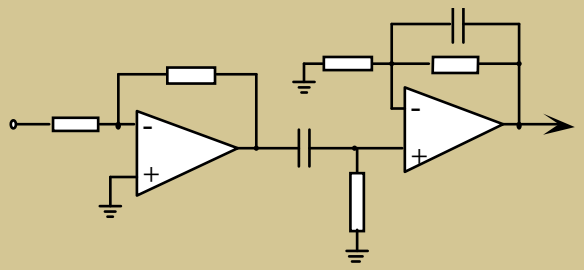
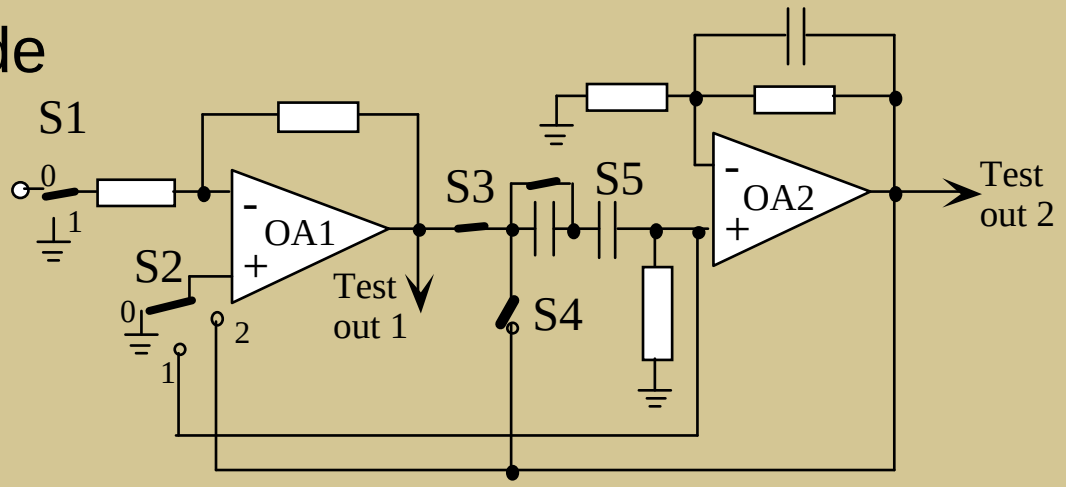
Design for Testability and Built-in Self-Test

Functional reconfiguration based schemes

- Oscillation test mode





	S1	S2	S3	S4	S5	Test out	Components tested
Normal mode	0	0	on	off	on		
Test mode f1	1	2	on	off	on	2	all
Test mode f2	1	2	on	off	off	2	all, but C1
Test mode f3	1	1	on	off	on	1	R1,R2,R3,C1,OA1
Test mode f4	1	1	on	off	off	1	R1,R2,R3,OA1
Test mode f5	1	0	off	on	on	2	R3,R4,R5,C1,C2,OA1,OA2
Test mode f6	1	0	off	on	off	1	R1,R2,R3,OA1

Testing Analog and Mixed-Signal Integrated Circuits Using Oscillation-Test Method
K. Arabi, B. Kaminska
IEEE Transactions on CADICS, vol.16,no.7,July 1997

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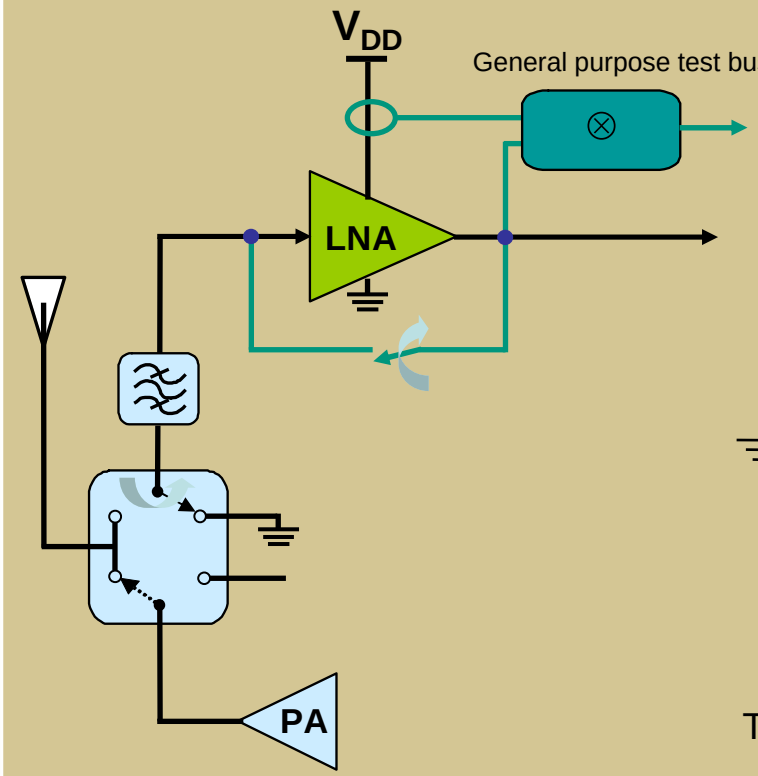
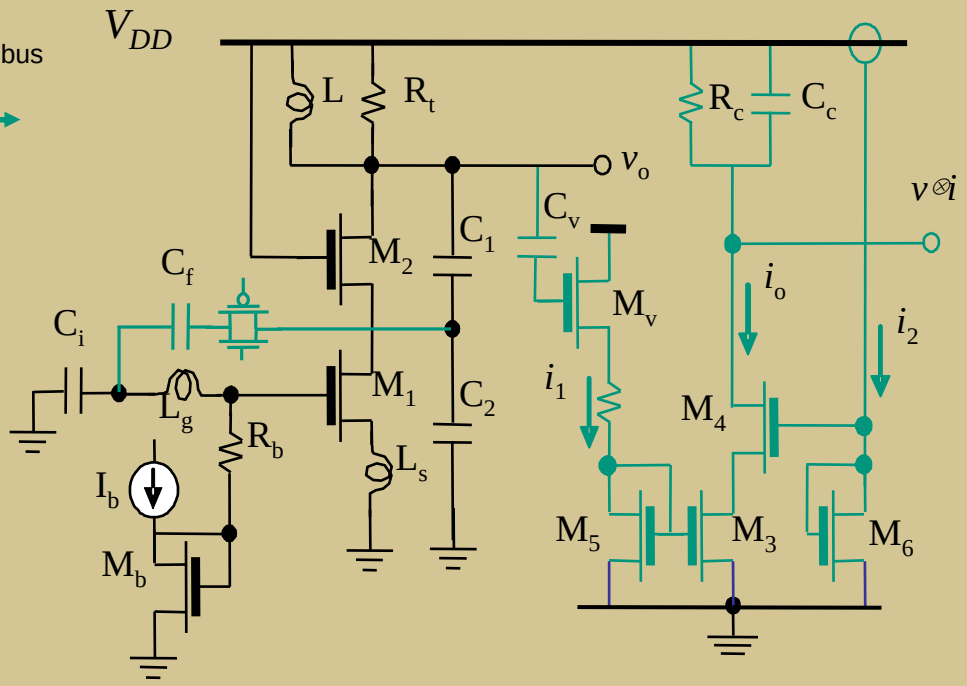
Design for Testability and Built-in Self-Test

Functional reconfiguration based schemes

- Oscillation test mode





The extra transistors' area overhead is smaller than 25%.

A Low-Power Oscillation Based LNA BIST Scheme
José Machado da Silva, Proceedings DTIS, 2006

DfT and BIST

Design for Testability and Built-in Self-Test

Catastrophic faults

Par. / Tol.	S11 -15↔-20	S12 -47↔-41	S21 19.5↔21.7	S22 -22↔-15	P1dB -18.5↔-13	NF 0.57↔0.61
1-M_{1gss}	-1	-175	-147	-24	-40	147
2-M_{1gds}	-1		2	-4	3.8	14.6
3-L_{gs}	-1	-54	7.2	-18	-7.6	6
4-L_{ss}						
5-M_{2gss}	-10	-214	-144	-24	-37	144
6-M_{2dss}	-7	-29.3	5.5	-5	>5	0.87
7-M_{2gds}		-51	10.8	-5		0.82
8-M_{1go}	-1	-108	-47		>5	54
9-R_{bo}			18		-20.6	0.56
10-L_{so}	-0	-139	-127	-11	-26	127

Observing a single parameter does not ensure a reliable fault detection

DfT and BIST

Design for Testability and Built-in Self-Test

Catastrophic faults

Par. Tol.	$\Re v_{out}^F i_{DD}^F$ 1.14↔1.79 V
1-M_{1gss}	3.3
2-M_{1gds}	3.3
3-L_{gs}	3.3
4-L_{ss}	1.2
5-M_{2gss}	
6-M_{2dss}	3.3
7-M_{2gds}	3.3
8-M_{1go}	3.3
9-R_{bo}	3.3
10-L_{so}	3.3

DfT and BIST

Design for Testability and Built-in Self-Test

Parametric

faults

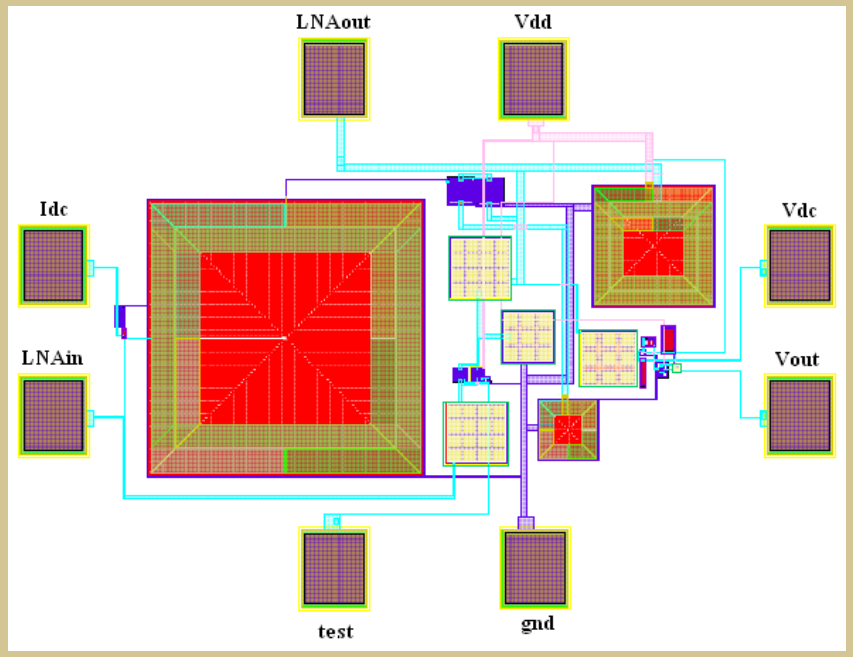
Par. / Tol.	S11 -15↔-20	S12 -47↔-41	S21 19.5↔21.7	S22 -22↔-15	P1dB -18.5↔-13	NF 0.57↔0.61
11-L_{g+20}	-8				-6.3	0.55
12-L_{g+10}					-10.7	0.55
13-L_{g-10}	-9					0.67
14-L_{g-20}	-5		18.8			0.77
15-L_{s+20}						
16-L_{s+10}						
17-L_{s-10}	-26					
18-L_{s-20}				-43		
19-L_{t+20}				-13		
20-L_{t+10}				-24		
21-L_{t-10}	-23			-8		
22-L_{t-20}	-21		18.3	-4		
23-C_{t+20}						
24-C_{t+10}						
25-C_{t-10}	-22			-9		
26-C_{t-20}	-23			-6		
27-M_{1+20}	-9				-8.2	0.55
28-M_{1+10}	-21				-10.5	0.55
29-M_{1-10}	-8				-19.8	0.67
30-M_{1-20}	-4			-14	-20	0.82
31-M_{2+20}				-25		
32-M_{2+10}						
33-M_{2-10}	-21			-14		
34-M_{2-20}				-13		

DfT and BIST

Design for Testability and Built-in Self-Test

Parametric faults

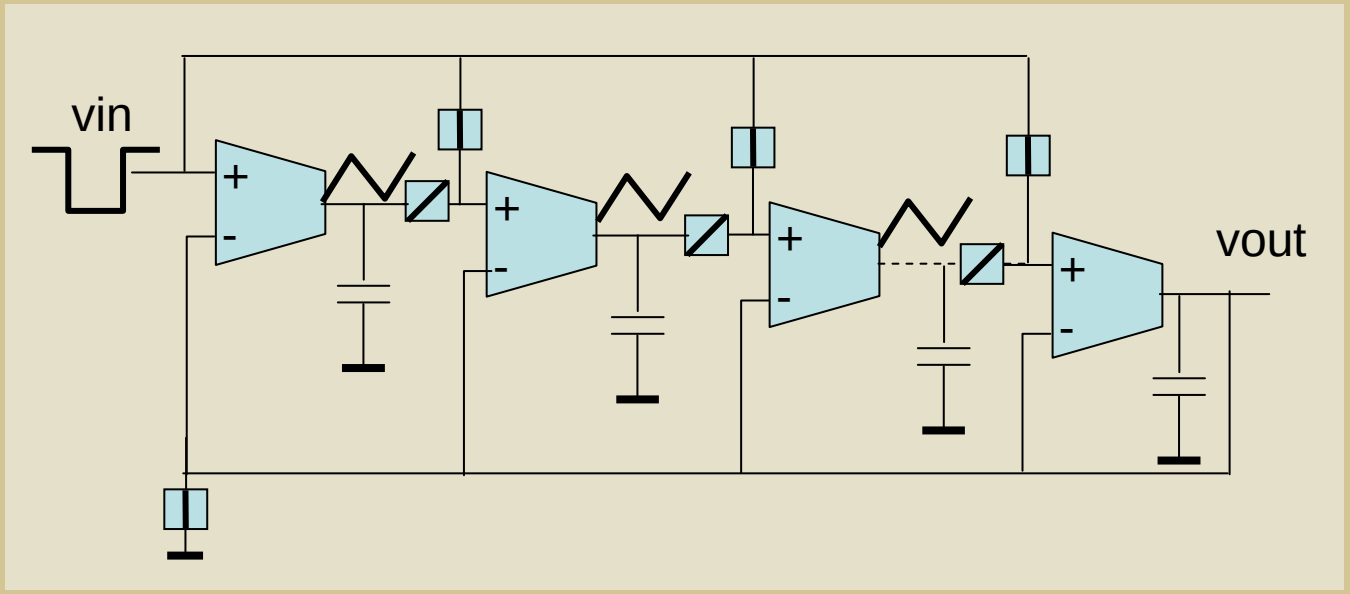
Par. Tol.	$\Re v_{out}^{F} i_{DD}^{F}$ 1.14↔1.79 V
12-L_{g+10}	0.3
13-L_{g-10}	1.9
14-L_{g-20}	3.3
15-L_{s+20}	2.2
16-L_{s+10}	1.6
17-L_{s-10}	
18-L_{s-20}	0.25
19-L_{t+20}	1.7
20-L_{t+10}	
21-L_{t-10}	
22-L_{t-20}	0.63
23-C_{t+20}	1.6
24-C_{t+10}	
25-C_{t-10}	
26-C_{t-20}	
27-W_{1+20}	0.3
28-W_{1+10}	0.4
29-W_{1-10}	1.85
30-W_{1-20}	3.3
31-W_{2+20}	1.43
32-W_{2+10}	1.3
33-W_{2-10}	
34-W_{2-20}	



DfT and BIST

Design for Testability and Built-in Self-Test

- **Functional reconfiguration based schemes**



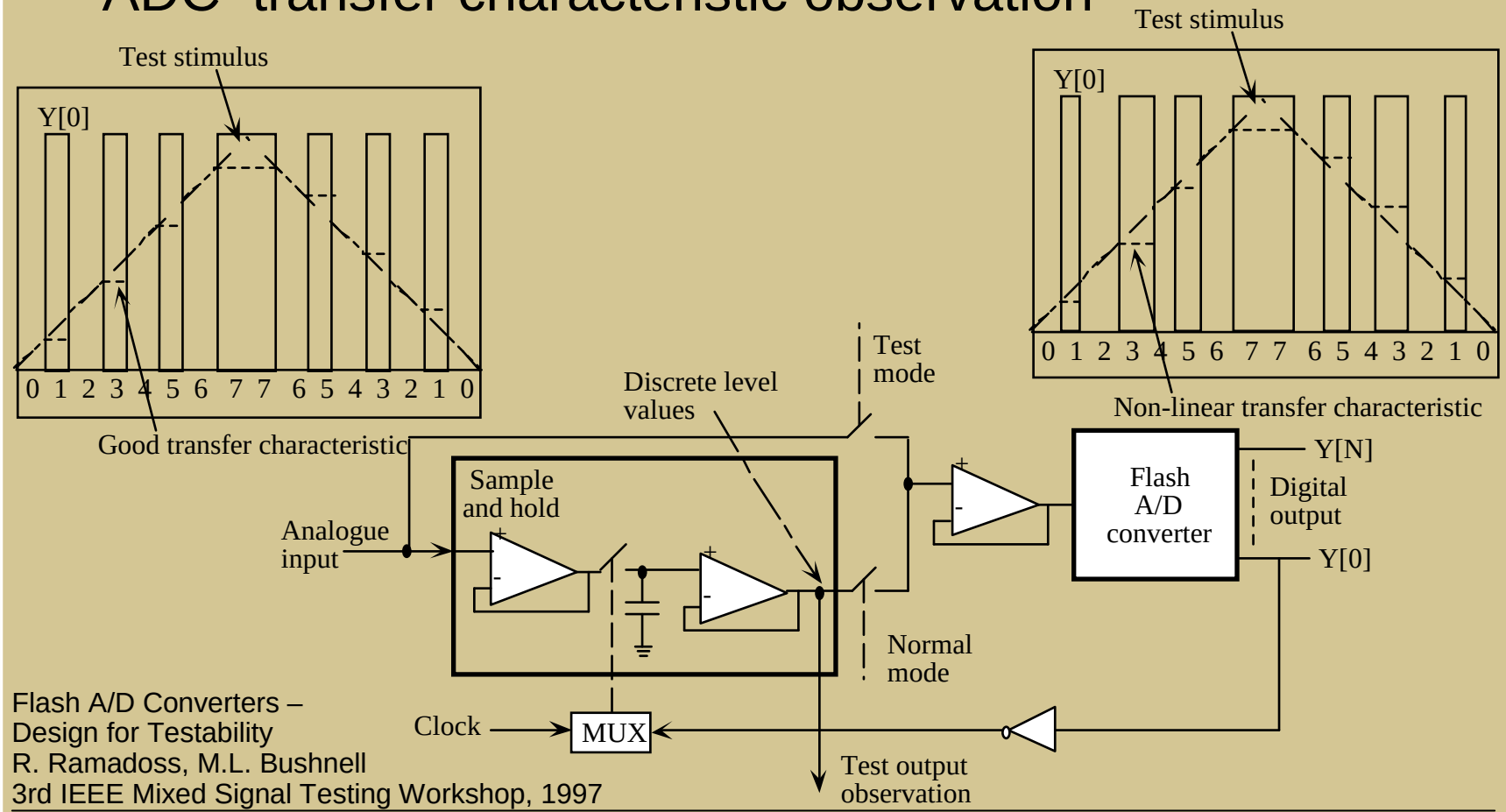
Testable Design of Multiple-Stage OTA-C Filters
Cheng-Chung Hsu and Wu-Shiung Feng,
IEEE TRANSACTIONS ON INSTRUMENTATION AND MEASUREMENT, VOL. 49, NO. 5, OCTOBER 2000

DfT and BIST

Design for Testability and Built-in Self-Test

Functional reconfiguration based schemes

- ADC transfer characteristic observation



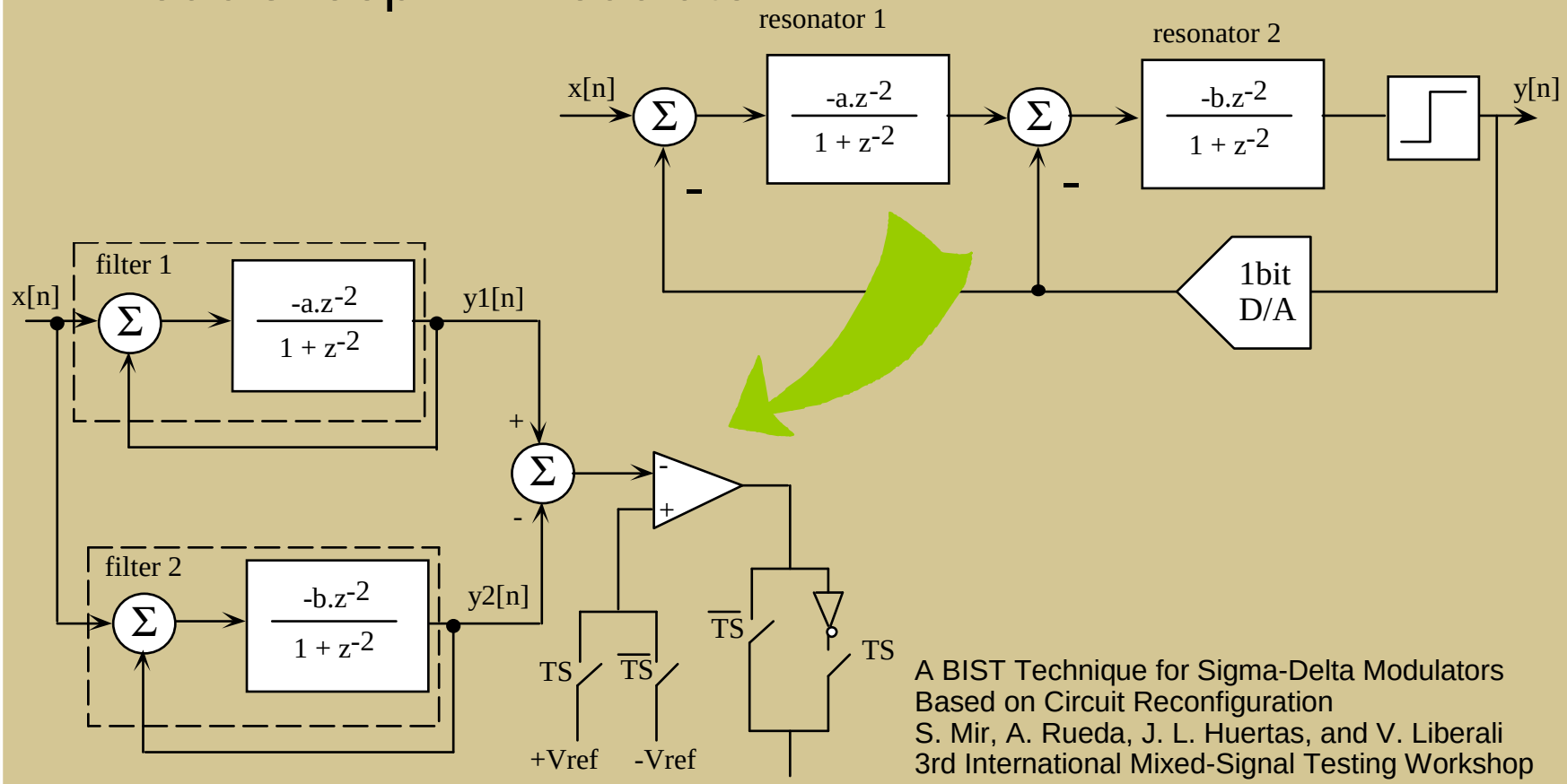
Flash A/D Converters – Design for Testability
R. Ramadoss, M.L. Bushnell
3rd IEEE Mixed Signal Testing Workshop, 1997

DfT and BIST

Design for Testability and Built-in Self-Test

Functional reconfiguration based schemes

- Double-loop ΣΔ modulator



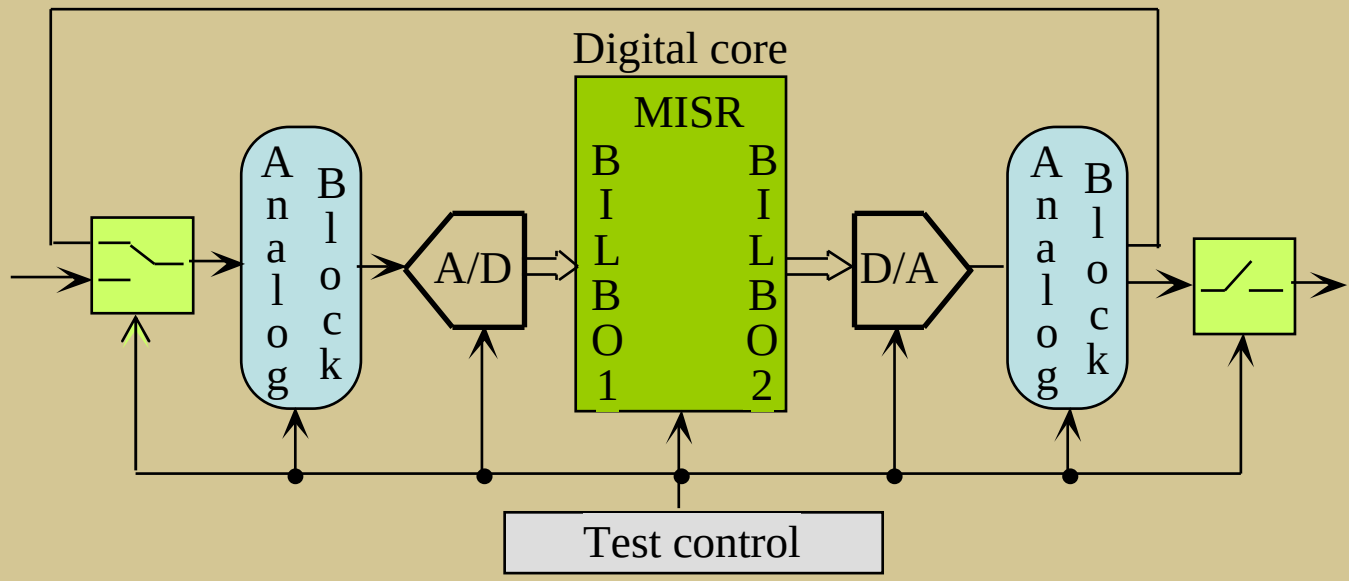
A BIST Technique for Sigma-Delta Modulators Based on Circuit Reconfiguration
S. Mir, A. Rueda, J. L. Huertas, and V. Liberali
3rd International Mixed-Signal Testing Workshop

DfT and BIST

Design for Testability and Built-in Self-Test

Functional reconfiguration based schemes

- Hybrid BIST

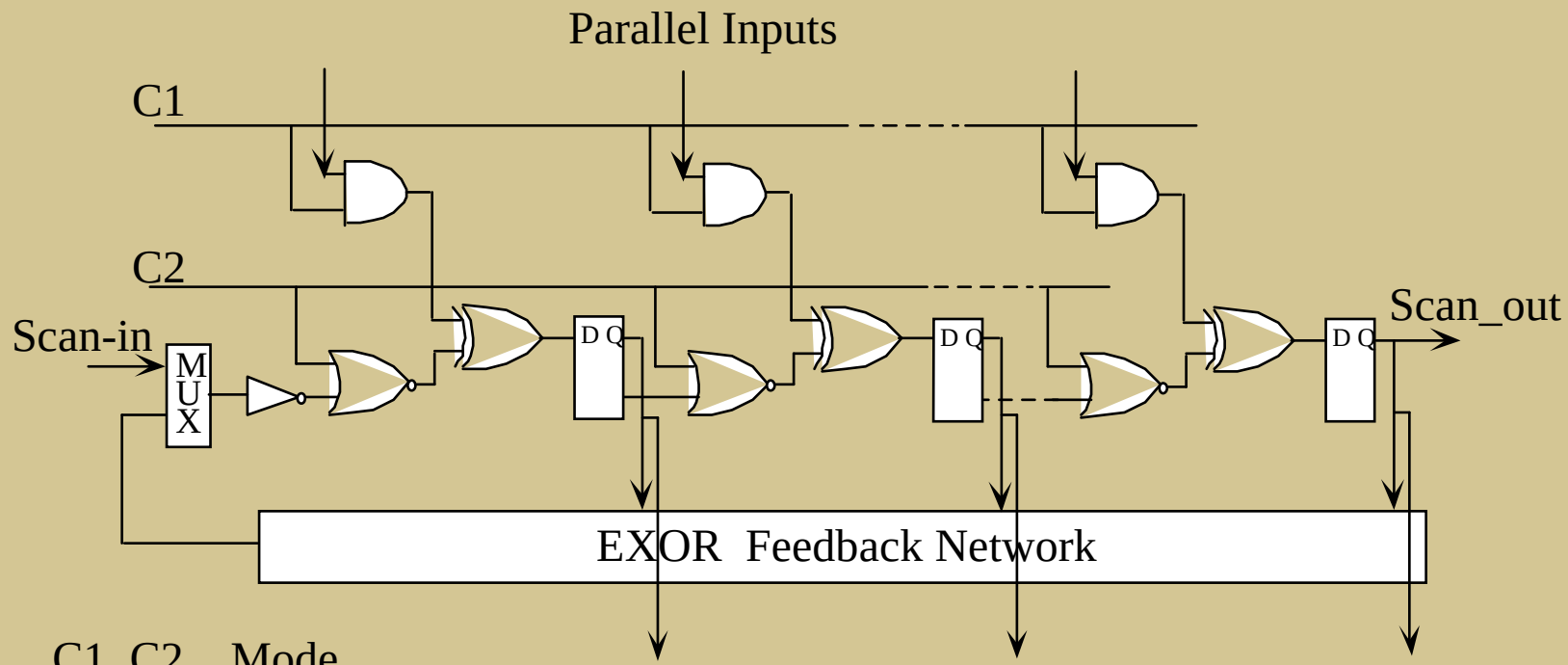


Hybrid Built-in self-test (HBIST) for mixed analogue/digital integrated circuits
M. J. Ohletz, Proceedings of the 2nd European Test Conference, April 1991

DfT and BIST

Design for Testability and Built-in Self-Test

Built-in Logic Block Observer



C1	C2	Mode
0	0	Scan
0	1	Clear
1	0	MISR
1	1	Normal

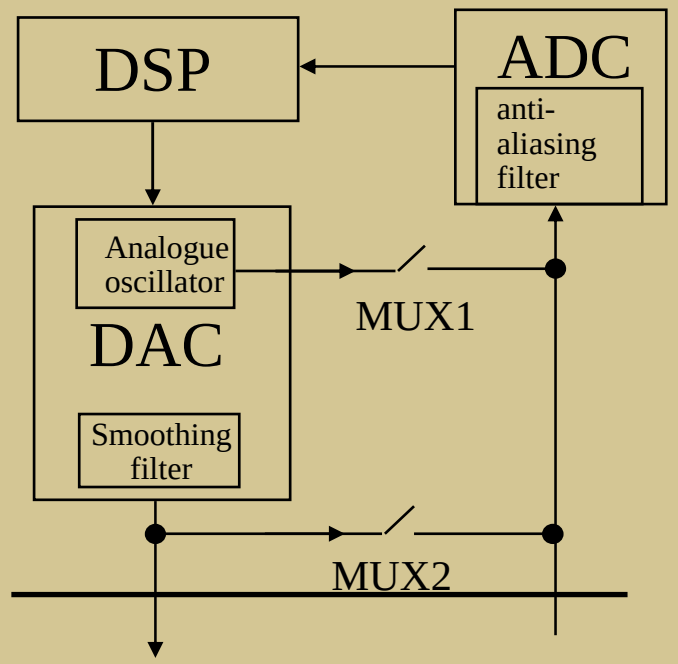
Built-in logic block techniques
B. Koenemann, J. Mucha, G. Zwiehof
Proc. International Test Conference, 1979

DfT and BIST

Design for Testability and Built-in Self-Test

Functional reconfiguration based schemes

- MADBIST



A BIST Scheme for an SNR test of a Sigma-Delta ADC
M.F. Toner, and G.W. Roberts
Proceedings of International Test Conference, 1993

1 - fully digital test
2 - convert D/A to oscillator (without smoothing filter)
3 - close Mux1
4 - test ADC
5 - DAC set to normal operation
6 - DAC can be tested after closing Mux2
7 - use DSP computational resources to implement a narrow band digital filter which allows computing parameters such as SNR and IMD

DfT and BIST

Design for Testability and Built-in Self-Test

- Mixed-signal BIST hurdles
  - Lack of robust traceability to central standards such as NIST
  - Designs are very close to specification limits requiring great accuracy in measurements
  - The use of on-chip stimulus and measurement circuits throws doubt into the accuracy of measurements, since there is a question about the quality of the signals generated and measured on a given DUT

DfT and BIST

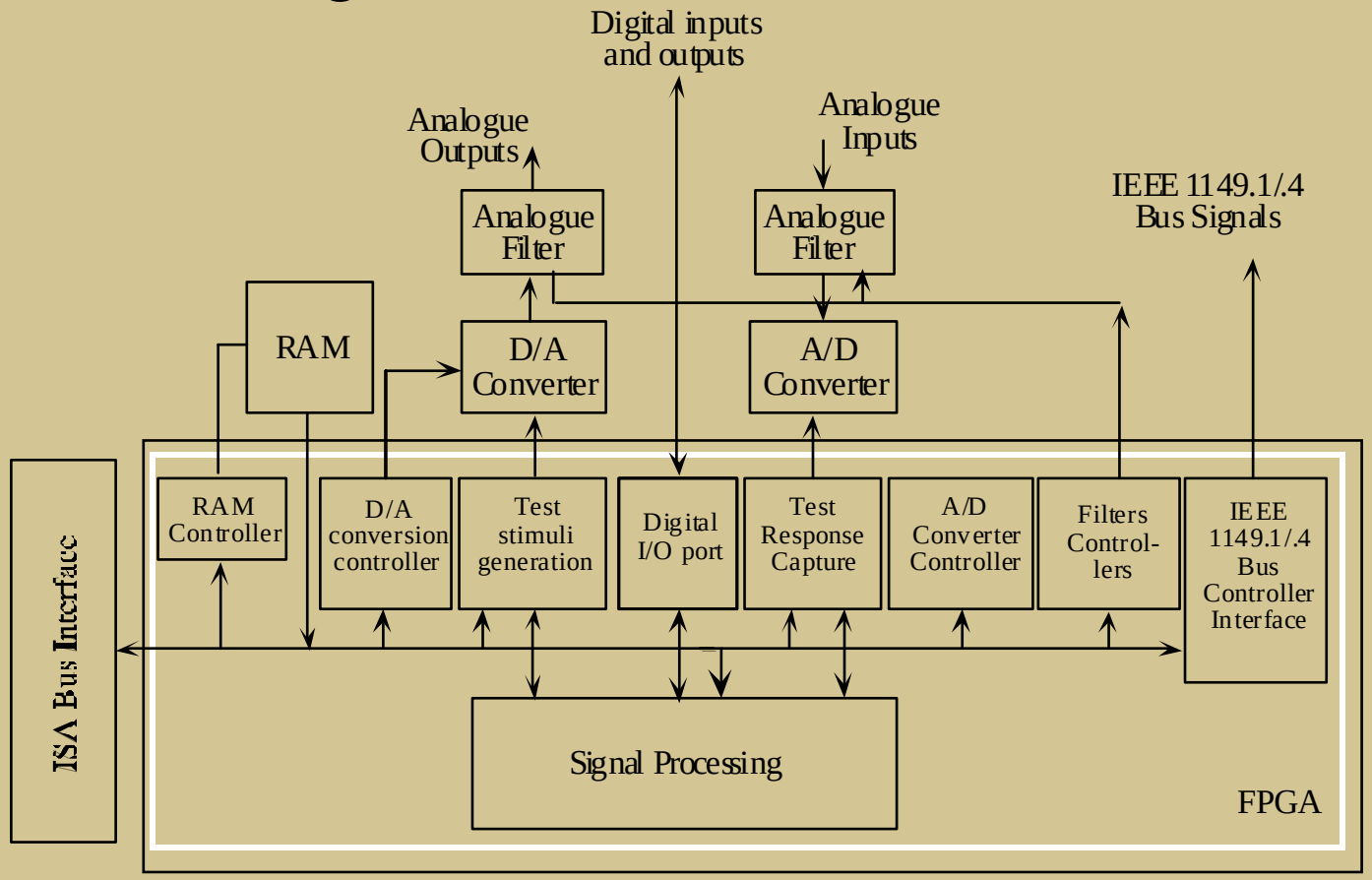
Design for Testability and Built-in Self-Test

- BIST instrumentation is often inferior to ATE equipment
  - ATE is calibrated, traceable to NIST
  - ATE digitizers & sources include anti-aliasing and anti-imaging circuits
  - Circuit overhead to implement BIST is overwhelming unless circuits are already present in design (microprocessor, DSP, ADC, DAC etc)
  - Problems are not insurmountable, but mixed-signal BIST can't be applied blindly

DfT and BIST

Design for Testability and Built-in Self-Test

Re-use of existing resources

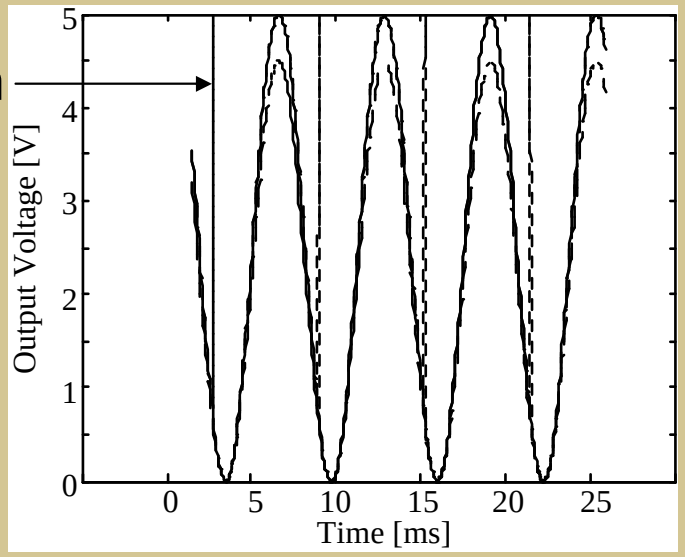


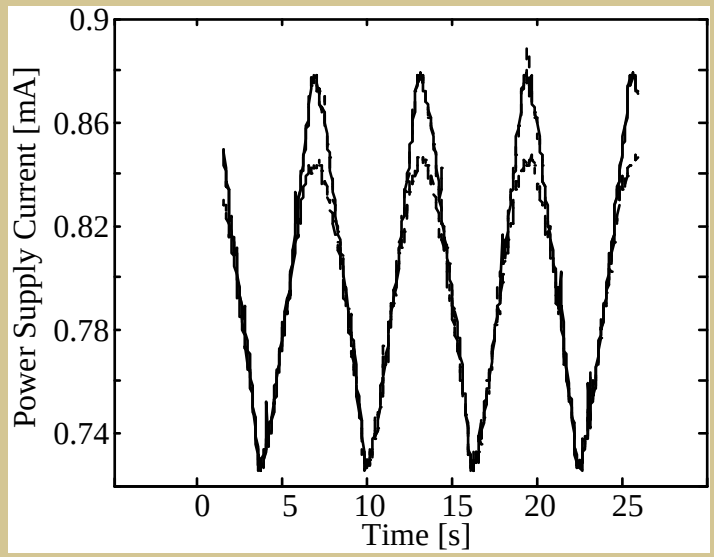
José M. Silva, J. S. Duarte, and José S. Matos, "Mixed-Signal BIST Using Correlation and Reconfigurable Harware", Design, Automation and Test in Europe Conference, DATE 2000.

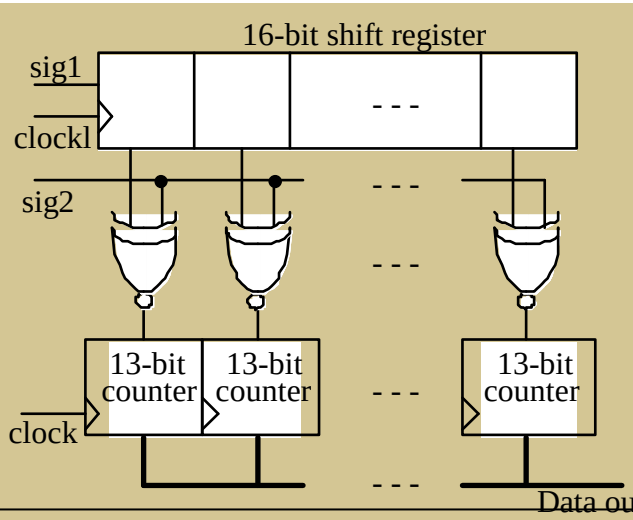
DfT and BIST

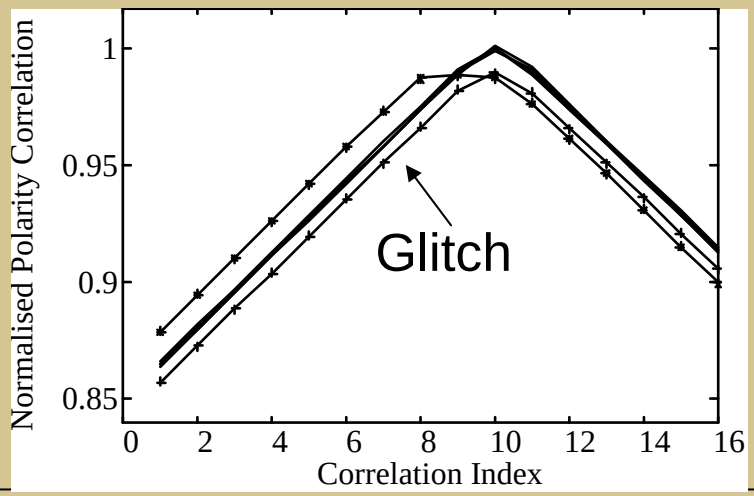
Design for Testability and Built-in Self-Test

Glitch





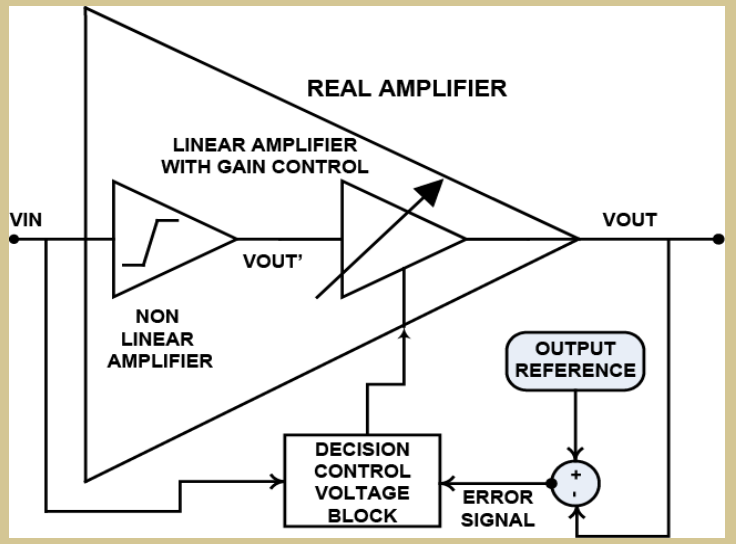


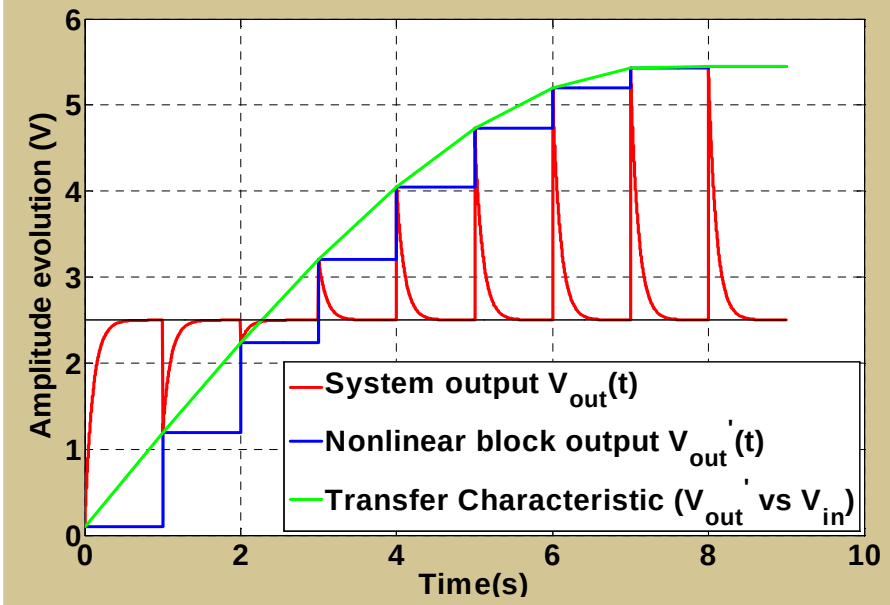


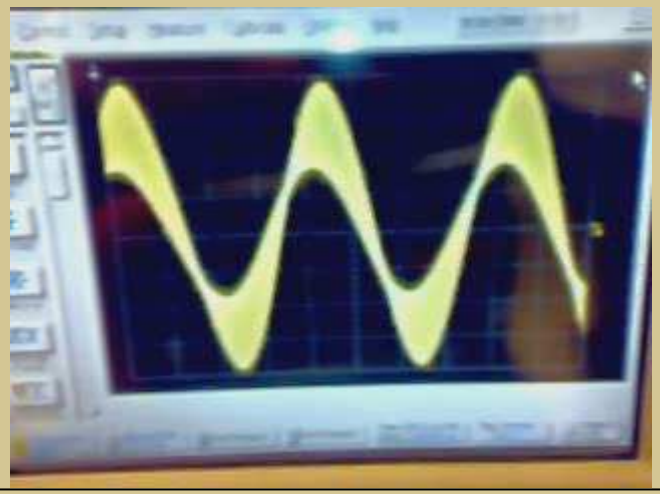
DfT and BIST

Design for Testability and Built-in Self-Test

- **Estimation of the amplifier's nonlinearity.**
- **Automatic gain control**
- **Correction of eye diagrams' opening**







"An Adaptive Scheme for Estimating and Correcting RF Amplifiers' Non-Linearities"
Pedro Mota, José Machado da Silva
APCCAS, 2008

Test and Design for Testability of Analog and Mixed-Signal Circuits

ACEOLE - PH-ESE Electronics Seminars

4-5 February 2010

José Machado da Silva

U.Porto – Faculdade de Engenharia

INESC Porto